Organization_____ Bldg./Room_____

U. S. DEPARTMENT OF COMMERCE
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
IF UNDELIVERABLE RETURN IN TEN DAYS

OFFICIAL BUSINESS

AN EQUAL OPPORTUNITY

ARLINGTON VA

U.S. OFFICIAL MAIL
U.S. POSTAGE
PENALTY FOR PRIVATE USE $300
09.75

GINS907 926601032 1403 25 08/21/04
FORWARD TIME EXP RTN TO SEND
GINSBERG
21 SAN ANTONIO
NEWPORT BEACH CA 92660-9112

RETURN TO SENDER

12

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,716	03/14/2001	Xianbin Wang	21046.P008	5815

7590 08/17/2004

Lawrence N. Ginsberg
907 Citrus Place
Newport Beach, CA 92660

EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	5

DATE MAILED: 08/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,716	WANG ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-18 and 33-35* is/are allowed.

6)☒ Claim(s) *19-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 20-XXX are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 20, 22 and 25-26 recite the limitation "the hybrid attenuator" in line 2. There is insufficient antecedent basis for this limitation in the claim.

4. Claims 21, 23-24 and 27-30 are likewise rejected because they depend on a base rejected claim.

5.

6. Claim 26 recites the limitation "the non-linear attenuator" in line 6. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 27 recites the limitation "the second digital non-linear attenuator" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

8. Claims 28-30 are likewise rejected because they depend on a base rejected claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 19 and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Ghanadan et al U.S. patent No 6,294,956 B1.

As per claim 19, Ghanadan et al teaches a receiver for a multi-carrier modulation (MCM) communication receiver comprising: a high power amplifier is the same as the claimed (hybrid amplifier) (see figs.15, 17-20 elements 102, 104, 142, 144, 180, 182, 210-216, 274, 276 and col.1, lines 40-41 and col.7, lines 5-7) having an input for receiving a PAPR reduced MCM signal, the PAPR reduced MCM signal comprising a plurality of PAPR reduced data samples, wherein each of the plurality of PAPR reduced data samples comprise an amplitude value, and the hybrid amplifier having an output for providing a PAPR restored MCM signal comprising a plurality of PAPR restored data samples, wherein each of the plurality of PAPR restored data samples comprises a restored amplitude value (see col.2, lines 40-47 and col.3, lines 10-25 and col.5, lines 45-67 and col.6, lines 30-67 and col.7, lines 50-67 and col.8, lines 21-51 and col.9, lines 17-67 and col.12,lines 35-67 and col.13, lines 1-17 and col.14, lines 15-32 see also cols.16-19).

As per claims 31-32, Ghanadan et al does teach a digital signal processor (see col.12, line 51).

Allowable Subject Matter

11. Claims 1-18 and 33-35 are allowed over the prior art of record.

12. Claims 20-30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: The prior arts of record fail to anticipate or render obvious the following recited features: he hybrid amplifier for linearly amplifying the normalized amplitude values of at least some of the plurality of normalized data o samples when the amplitude values of the at least some of the plurality of normalized data samples satisfy the predetermined amplitude value criteria, and the hybrid amplifier for non-linearly amplifying normalized amplitude values of some other of the plurality of normalized data samples when the normalized amplitude values of the at least some 5 other of the plurality of normalized data samples do not satisfy the predetermined amplitude criteria, and for producing a plurality of amplified amplitude values, the hybrid amplifier having an output for providing a MCM signal comprising the plurality of amplified amplitude values as recited in claim 1. Attenuating the amplitude value of the received amplified amplitude values non-linearly in accordance with a first non-linear function when the received amplified amplitude values are greater than the maximum amplitude value; comparing the amplified amplitude values with the minimum amplitude value; g) attenuating the amplified amplitude values non-linearly in 50 accordance with a second non-linear function when the amplified amplitude values are less than the minimum amplitude value; and providing a restored MCM signal comprising a plurality of PAPR restored data samples representing the linearly attenuated amplitude values, and the non-linearly attenuated amplitude values in accordance with the first and the second non-linear functions as recited in claims 33 and 35.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hamilton-Piercy et al U.S. patent No 5,809,395 teaches a remote antenna driver for radiotelephony system.

Frank et al U.S. patent No 6,636,555 B1 teaches an amplitude limitation.

Shastri et al U.S. patent No 6,128,350 teaches a method and apparatus for reducing peak to average power.

Luz U.S. patent No 5,783,969 teaches a method and system for preventing an amplifier overload condition.

Sarraf U.S. patent No 6,157,812 teaches a system and method for enhanced satellite payload.

McAlear U.S. patent No 6,598,232 B1 teaches a hybrid amplifier regenerator.

Feher U.S patent no 6,757,334 B1 teaches a bit rate agile third generation wireless CDMA.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 703 308-9573. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 703 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

8/11/04

EMMANUEL BAYARD
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 09/808,716	Applicant(s)/Patent Under Reexamination WANG ET AL.	
	Examiner Emmanuel Bayard	Art Unit 2631	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,757,334	06-2004	Feher, Kamilo	375/259
	B	US-6,598,232	07-2003	McAlear, James Allan	725/126
	C	US-6,157,812	12-2000	Sarraf, Jamal	455/13.4
	D	US-5,783,969	07-1998	Luz, Yuda Yehuda	330/124R
	E	US-6,128,350	10-2000	Shastri et al.	375/260
	F	US-6,636,555	10-2003	Frank et al.	375/146
	G	US-5,809,395	09-1998	Hamilton-Piercy et al.	725/106
	H	US-6,294,956	09-2001	Ghanadan et al.	330/124R
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

US006757334B1

(12) **United States Patent**
Feher

(10) **Patent No.: US 6,757,334 B1**
(45) **Date of Patent: Jun. 29, 2004**

(54) **BIT RATE AGILE THIRD-GENERATION WIRELESS CDMA, GSM, TDMA AND OFDM SYSTEM**

(76) Inventor: **Kamilo Feher**, 44685 Country Club Dr., El Macero, CA (US) 95618

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/370,362**

(22) Filed: **Aug. 9, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/095,943, filed on Aug. 10, 1998, and provisional application No. 60/098,612, filed on Aug. 31, 1998.

(51) **Int. Cl.**[7] **H04L 27/00**

(52) **U.S. Cl.** **375/259**; 375/219; 375/261; 375/296; 375/298

(58) **Field of Search** 375/130, 219, 375/259, 260, 261, 267, 298, 347, 296; 370/206, 208, 215; 455/115, 126, 132, 133, 134

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,944,926	A		3/1976	Feher ..... 325/38 R
4,103,234	A		7/1978	Frazier, Jr. ..... 325/38 A
4,339,724	A		7/1982	Feher 328/164
4,350,879	A		9/1982	Feher 235/92
4,403,331	A		9/1983	Halpern et al. 375/37
4,517,679	A		5/1985	Clark et al. 375/37
4,530,088	A		7/1985	Hamstra et al. 370/110.1
4,567,602	A	*	1/1986	Kato et al. 375/296
4,644,565	A		2/1987	Seo et al. 375/60
4,720,839	A		1/1988	Feher et al. 375/18
4,730,344	A		3/1988	Saha 375/53
5,327,455	A		7/1994	De Gaudenzi et al. 375/1
5,341,396	A	*	8/1994	Higgins et al. 375/130
5,365,547	A		11/1994	Marinaro 375/37
5,491,457	A		2/1996	Feher 332/103
5,719,899	A		2/1998	Thielecke et al. 375/206
5,729,570	A		3/1998	Magill 375/206
5,732,114	A		3/1998	Thebault et al. 375/368
5,784,402	A		7/1998	Feher 375/200
5,790,588	A		8/1998	Fukawa et al. 375/200
6,198,777	B1	*	3/2001	Feher 375/295
6,445,749	B2	*	9/2002	Feher 375/298
6,470,055	B1	*	10/2002	Feher 375/259

FOREIGN PATENT DOCUMENTS

CA	1130871	8/1982
CA	1211517	9/1986
CA	1265851	2/1990

OTHER PUBLICATIONS

Feher, K.: *Wireless Digital Communications: Modulation Spread Spectrum*. Prentice Hall, 1995.

Feherd, K.: *Digital Communications: Satellite/Earth Station Engineering*. Prentice Hall, 1983. Available from Crestone Engineering –Noble Publishing, 2245 Dillard Street, Tucker, Georgia 30084.

Feher, K.: *Advanced Digital Communications: Systems and Signal Processing*. Prentice Hall, 1987. Available from Crestone Eingineering –Noble Publishing, 2245 Dillard Street, Tucker, Georgia 30084.

Feher, K.: *Digital Communications: Microwave Applications*. Prentice Hall 1981. Since 1997 available from Crestone Eingineering –Noble Publishing, 2245 Dillard Street, Tucker, Georgia 30084.

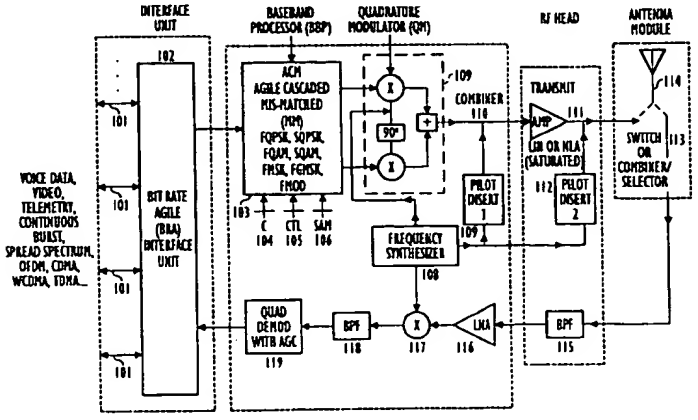
(List continued on next page.)

Primary Examiner—Shuwang Liu
(74) *Attorney, Agent, or Firm*—Dorsey & Whitney LLP

(57) **ABSTRACT**

Systems, apparatus, and methods for new generations of wireless systems, including multiple standard, interoperable Third-Generation (3G) and Second-Generation (2G), Spread Spectrum CDMA, WCDMA, GSM, Enhanced GSM systems and CSMA, TDMA and OFDM. Bit Rate Agile (BRA), Modulation and Code Selectable processing techniques of Gaussian Minimum Shiftl Keying (GMSK), Quadrature Phase Shift Keying (QPSK), Quadrature Amplitude Modulation (QAM), and of Mis-Matched demodulator filters in which the demodulator filter set is mis-matched to the filter set of the signal modulator.

4 Claims, 45 Drawing Sheets-



OTHER PUBLICATIONS

Feher, K. and Engineers of Hewlett–Packard: *Telecommunicatioris Measurements, Analysis, and Instrumentation*: Prentice Hall 1987 . Since 1997 reprints have been available from Crestone Engineering –Noble Publishing, 2245 Dillard Street, Tucker, Georgia 30084.

Feher, K., Emmenegger, H.: "FQPSK Use for Electronic News Gathering (ENG), Telemetry and Broadcasting," *Proc. of the National Association of Broadcasters* NAB'99 Broadcast Engineering Conference, Las Vegas, Apr. 19–22, 1999.

Feher, K.: "FQPSK Doubles Spectral Efficency of Operational Systems: Advances, Applications, Laboratory and Initial Air–to–Ground Flight Tests" (Date of Submission: Aug. 14, 1998). *Proc. of the International Telemetry Conference*, ITC–98 ITC/USA 98, San Diego, CA, Oct. 26–29, 1998.

W. Gao, S.H. Wang, K. Feher: "Blind Equalization for FQPSK and FQAM Systems in Multipath Frequency Selective Fading Channels," *Proc. Internat. Telemetry Conf.* ITC/USA'99, Oct. 25–28, 1999, Las Vegas, NV.

Terziev, G., Feher, K.: "Adaptive Fast Blind Feher Equalizers (FE) for FQPSK," *Proc. Of the International Telemetry Conference* ITC/USA'99, Oct. 25–28, 1999, Las Vegas, Nevada.

Feher, K.: "FQPSK Transceivers Double the Spectral Efficiency of Wireless and Telemetry Systems" *Applied Microwave & Wireless Journal*, Jun. 1998.

Seo, J–S. and K. Feher: "Bandwidth Compressive 16–State SQAM Modems through Saturated Amplifiers," *IEEE Radio Commun.*, ICC '86, Toronto, Jun. 1986.

Kato, S. and K. Feher: "XPSK: A new cross–correlated PSK," *IEEE Trans. Com.*, May 1983.

Law, E.L., U.S. Navy: "Robust Bandwidth Efficient Modulation" *European Telemetry Conference, ETC–98*, Germany, May 1998.

Feher, K.: "FQPSK Doubles the Spectral Efficiency . of Operational Telemetry Systems," *European Telemetry Conference, ETC–98*, May 1998, Germany.

Do, G. and K. Feher: "FQPSK–GMSK: Wireless System Tests an ACI Environment," *Proc. of Wireless Symposium*, Santa Clara, CA, Feb. 9–13, 1998.

Law, E. and K. Feher: "FQPSK versus PCM/FM for Aeronautical Telemetry Applications: Spectral Occupancy and Bit Error Probability Comparisons" *Proc. of ITC–97*, Las Vegas, Oct. 1997.

Feher, K "FQPSK Doubles Spectral Efficiency of Telemetry: Advances and Intial Air to Ground Flight Tests," ITC/USA 98, *Proc. of the Internat. Telemetry Conference*, San Diego, Oct. 1998.

Law, E. and K. Feher: "FQPSK versus PCM/FM for Aeronautical Telemetry Applications; Spectral Occupancy and Bit Error Probability Comparisons," *Proc. of the Internat. Telemetry Conf.*, Las Vegas, Nevada, Oct. 27–30, 1997.

Martin, W.L., T–Y. Yan, L.V. Lam: "Efficient Modulation Study at NASA/JPL," *Proc. of the Tracking, Telemetry & Command Systems Confernce*, European Space Agency (ESA), Jun. 1998.

Law, E.L., ITC–98 Session Chair: "RCC Alternate Standards and IRIG106 update," Briefings by DoD during ITC/USA 98 *Internat. Telemetry Conference*, San Diego, Oct. 1998.

K. Feher: "FQPSK Doubles Spectral Efficiency of Operational Systems: Advances, Applications, Laboratory and Initial Air to Ground Flight Tests", File: ITC.98.Final Paper. Rev. Aug. 14, 1998 (Date of Submission) for publication in *the Proc. of the international Telemetering Conference*ITC–98; San DIego, Oct. 26–29, 1998.

Simon, M.K, Yan, T.Y. "Performance Evaluation and Interpretation of Unfiltered Feher–Patented Quadrature Phase–Shift Keying (FQPSK)," California Institute of Technology, JPL–NASA publication, *TMD Progress Report 42–137*, Pasadena, CA, May 15, 1999.

Winters, J.H. : "Adaptive Antenna Arrays for Wireless Systems," *Tutorial Notes presented/distributed at the 1999 IEEE Vehicular Technology Conference*, Houston, TX, May 16, 1999.

* cited by examiner

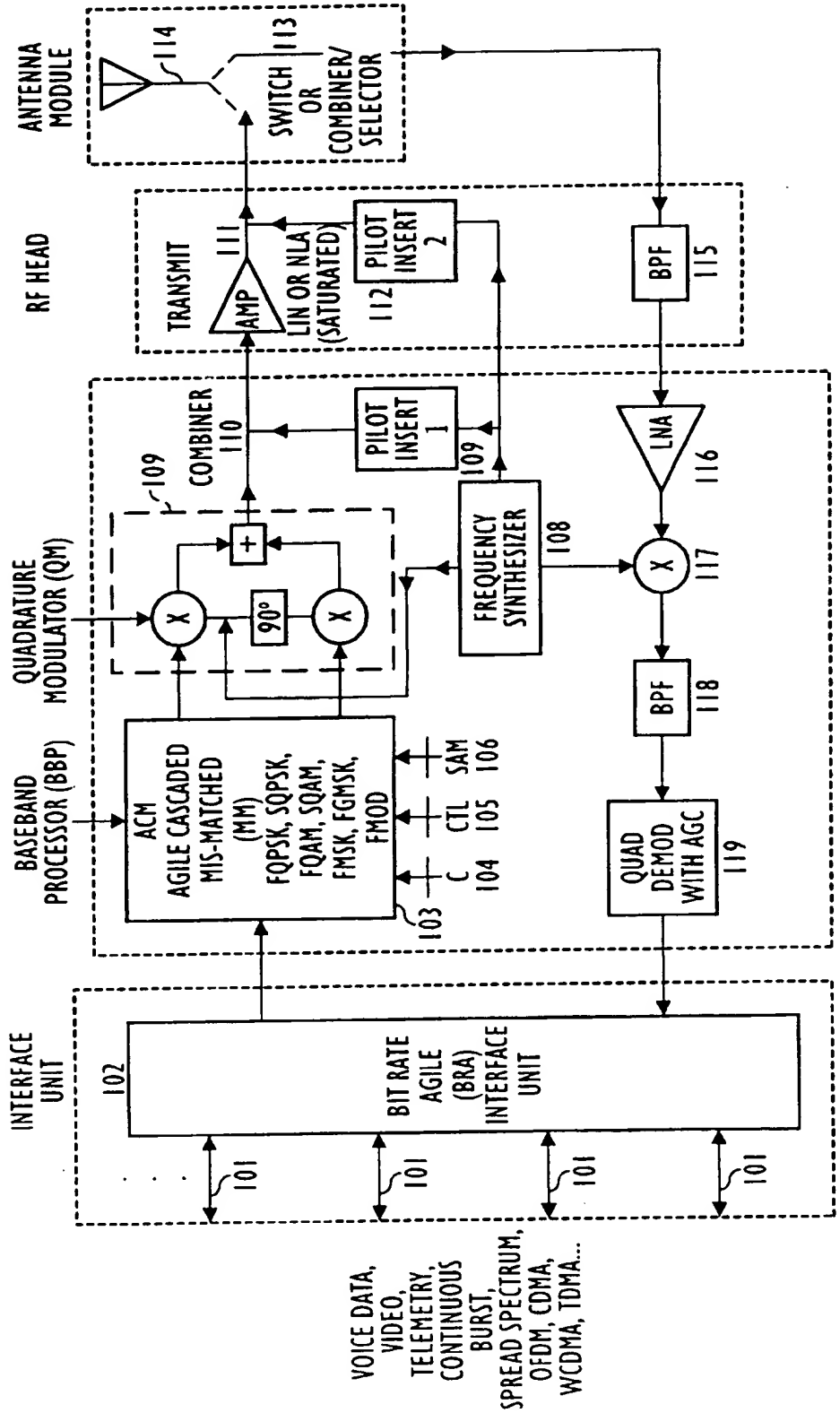

ANTENNA MODULE
114
SWITCH OR COMBINER/ SELECTOR
113
RF HEAD
TRANSMIT
111
AMP
LIN OR NLA (SATURATED)
PILOT INSERT 2
112
BPF
115
COMBINER
110
PILOT INSERT 1
109
LNA
116
109
QUADRATURE MODULATOR (QM)
90°
FREQUENCY SYNTHESIZER
108
117
BPF
118
BASEBAND PROCESSOR (BBP)
ACM AGILE CASCADED MIS-MATCHED (MM) FQPSK, SQPSK, FQAM, SQAM, FMSK, FGMSK, FMOD
SAM 106
CTL 105
C 104
103
QUAD DEMOD WITH AGC
119
INTERFACE UNIT
102
BIT RATE AGILE (BRA) INTERFACE UNIT
101
VOICE DATA, VIDEO, TELEMETRY, CONTINUOUS BURST, SPREAD SPECTRUM, OFDM, CDMA, WCDMA, TDMA...

FIG. 1A

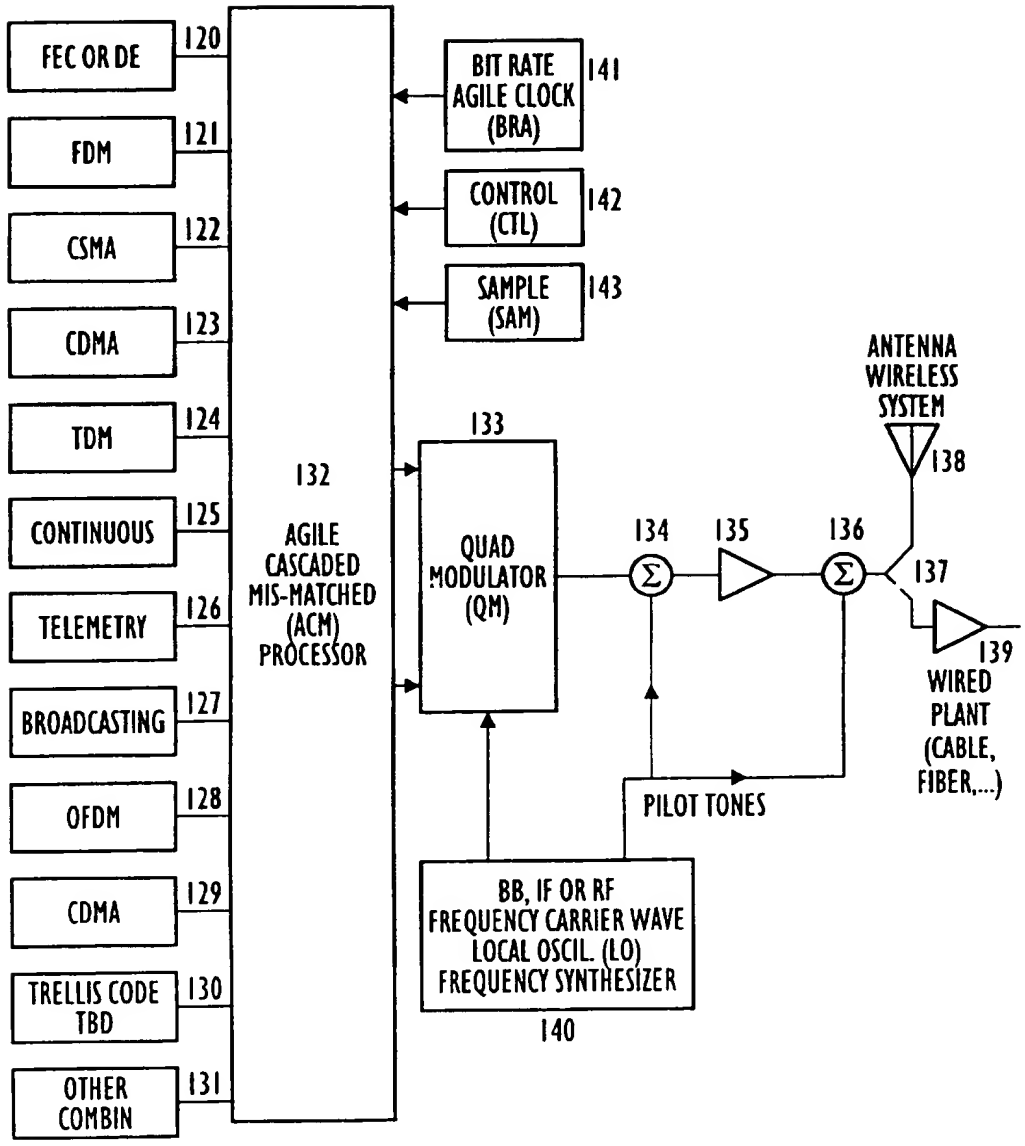

FEC OR DE
120
FDM
121
CSMA
122
CDMA
123
TDM
124
CONTINUOUS
125
TELEMETRY
126
BROADCASTING
127
OFDM
128
CDMA
129
TRELLIS CODE TBD
130
OTHER COMBIN
131
132
AGILE CASCADED MIS-MATCHED (ACM) PROCESSOR
BIT RATE AGILE CLOCK (BRA)
141
CONTROL (CTL)
142
SAMPLE (SAM)
143
133
QUAD MODULATOR (QM)
134
135
136
137
ANTENNA WIRELESS SYSTEM
138
139
WIRED PLANT (CABLE, FIBER,...)
PILOT TONES
BB, IF OR RF FREQUENCY CARRIER WAVE LOCAL OSCIL. (LO) FREQUENCY SYNTHESIZER
140

FIG. 1B

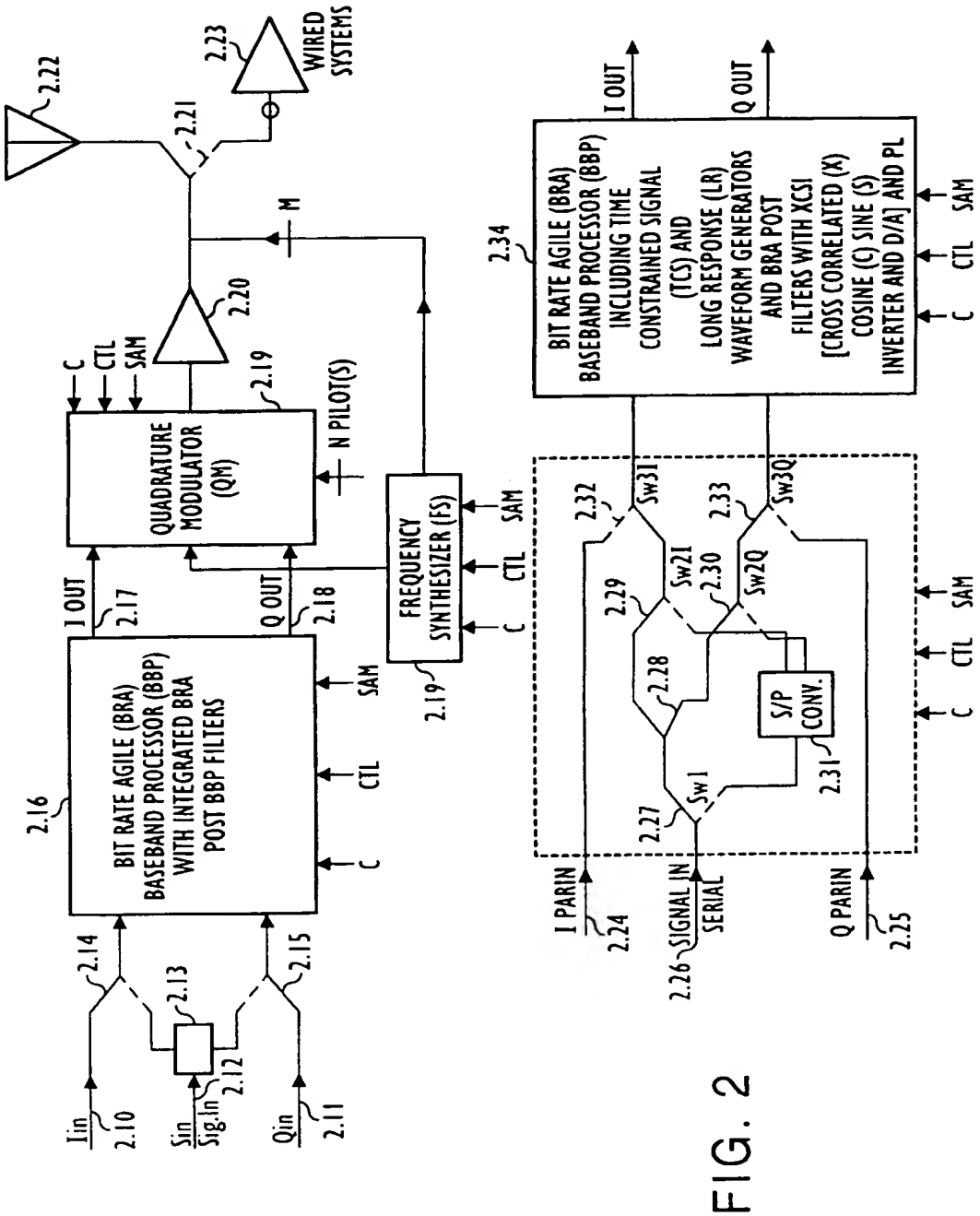

2.22
2.23
WIRED SYSTEMS
2.21
M
2.20
C
CTL
SAM
2.19
N PILOT(S)
QUADRATURE MODULATOR (QM)
I OUT
2.17
Q OUT
2.18
FREQUENCY SYNTHESIZER (FS)
2.19
C CTL SAM
2.16
BIT RATE AGILE (BRA) BASEBAND PROCESSOR (BBP) WITH INTEGRATED BRA POST BBP FILTERS
C CTL SAM
2.14
2.13
2.12
2.15
Iin
2.10
Sin
Sig.in
Qin
2.11
2.34
BIT RATE AGILE (BRA) BASEBAND PROCESSOR (BBP) INCLUDING TIME CONSTRAINED SIGNAL (TCS) AND LONG RESPONSE (LR) WAVEFORM GENERATORS AND BRA POST FILTERS WITH XCSI [CROSS CORRELATED (X) COSINE (C) SINE (S) INVERTER AND D/A] AND PL
I OUT
Q OUT
C CTL SAM
2.32
Sw31
2.33
Sw30
2.29
Sw21
2.30
Sw20
2.28
S/P CONV.
2.31
2.27
Sw1
I PARIN
2.24
SIGNAL IN SERIAL
2.26
Q PARIN
2.25
C CTL SAM

FIG. 2

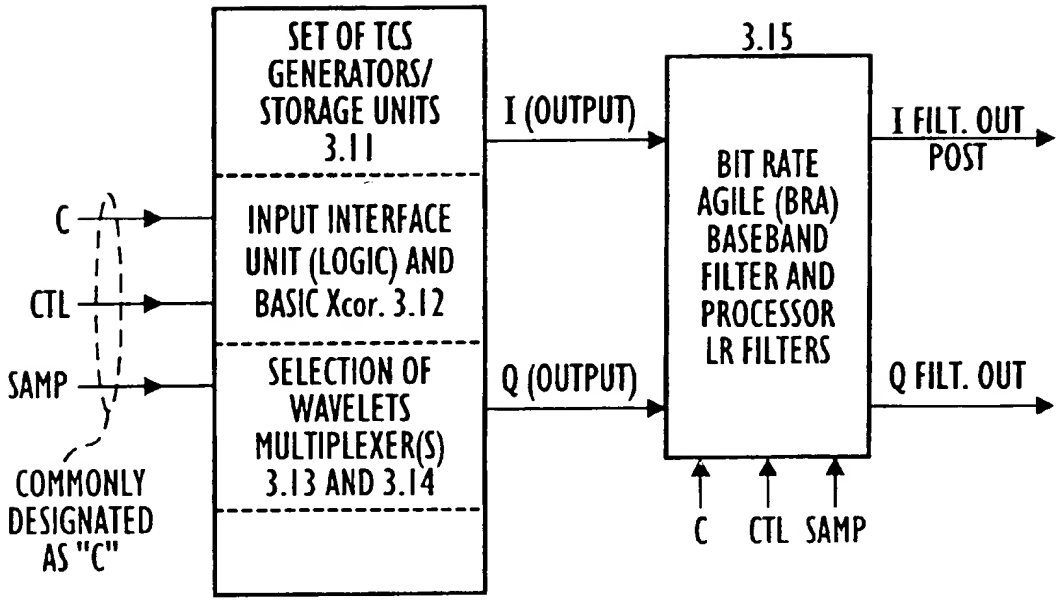

SET OF TCS GENERATORS/ STORAGE UNITS 3.11
INPUT INTERFACE UNIT (LOGIC) AND BASIC Xcor. 3.12
SELECTION OF WAVELETS MULTIPLEXER(S) 3.13 AND 3.14
C
CTL
SAMP
COMMONLY DESIGNATED AS "C"
I (OUTPUT)
Q (OUTPUT)
3.15
BIT RATE AGILE (BRA) BASEBAND FILTER AND PROCESSOR LR FILTERS
I FILT. OUT POST
Q FILT. OUT
C
CTL
SAMP

FIG. 3

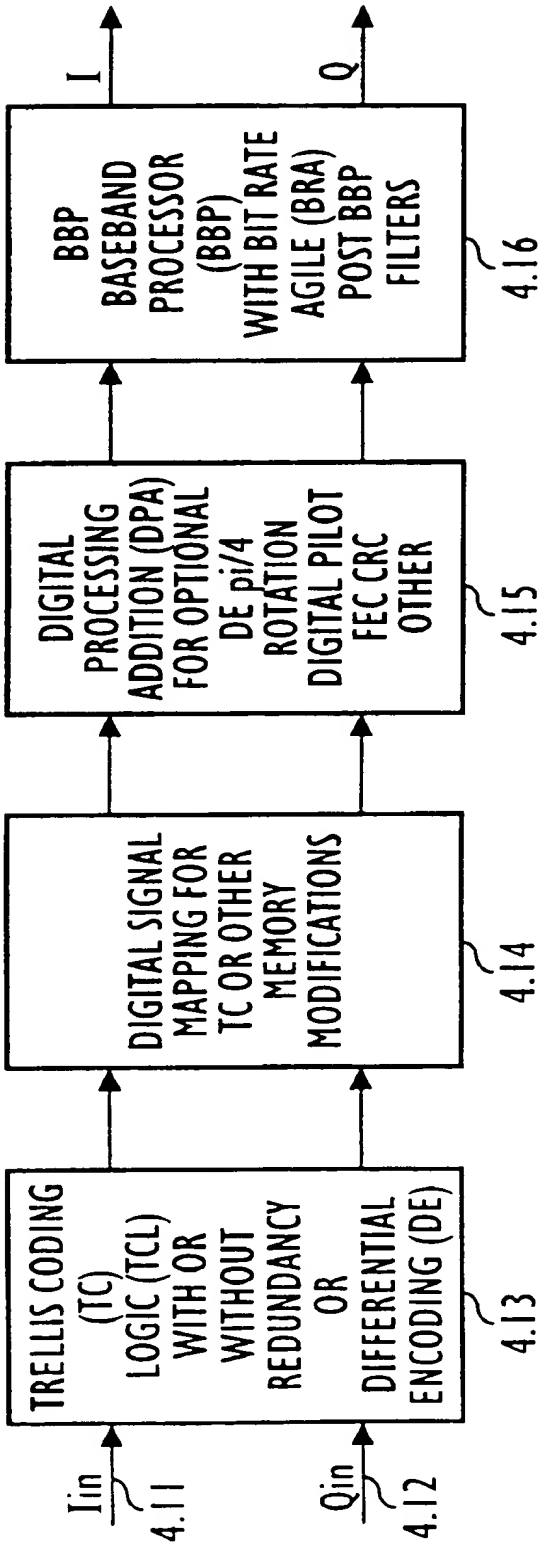

Iin
4.11
Qin
4.12
TRELLIS CODING (TC) LOGIC (TCL) WITH OR WITHOUT REDUNDANCY OR DIFFERENTIAL ENCODING (DE)
4.13
DIGITAL SIGNAL MAPPING FOR TC OR OTHER MEMORY MODIFICATIONS
4.14
DIGITAL PROCESSING ADDITION (DPA) FOR OPTIONAL DE pi/4 ROTATION DIGITAL PILOT FEC CRC OTHER
4.15
BBP BASEBAND PROCESSOR (BBP) WITH BIT RATE AGILE (BRA) POST BBP FILTERS
4.16
I
Q

FIG. 4

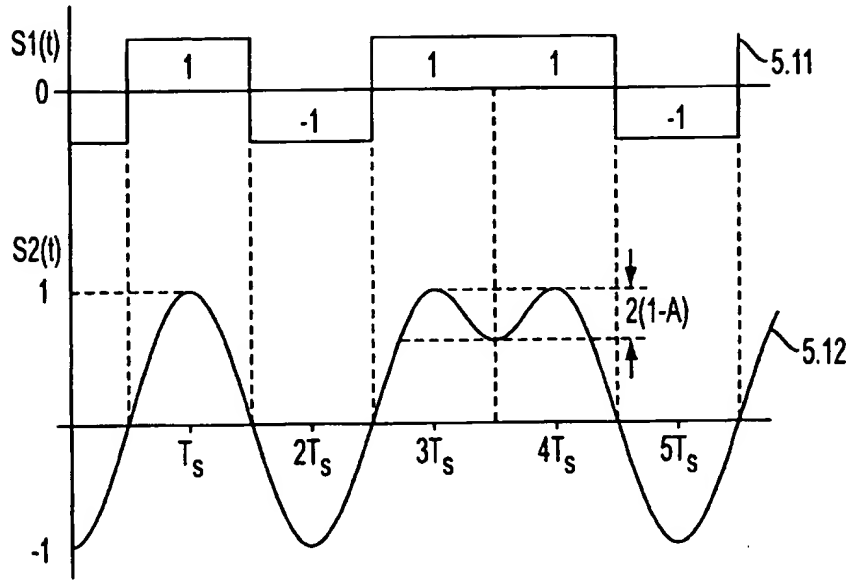


FIG. 5A

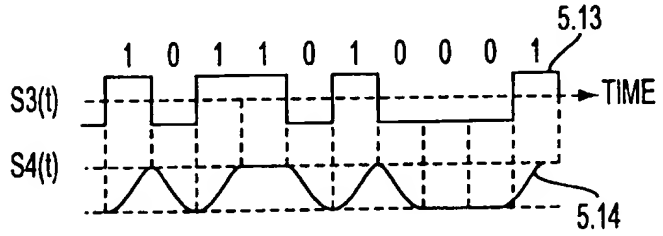


FIG. 5B

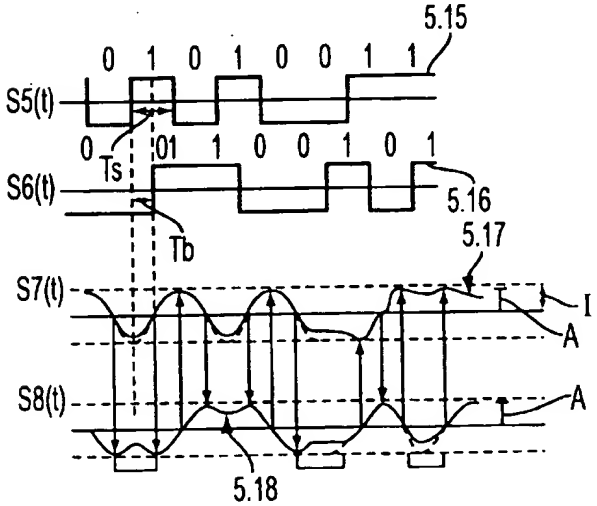


FIG. 5C

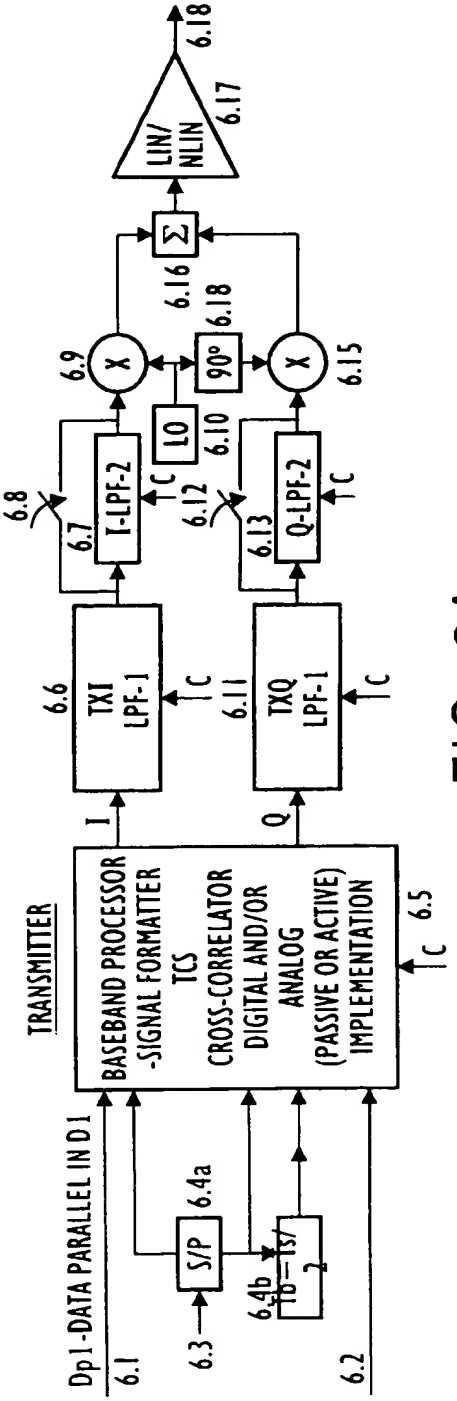

TRANSMITTER
Dp1-DATA PARALLEL IN D1
6.1
6.3
S/P
6.4a
6.4b
TD=1S/2
6.2
BASEBAND PROCESSOR
-SIGNAL FORMATTER
TCS
CROSS-CORRELATOR
DIGITAL AND/OR
ANALOG
(PASSIVE OR ACTIVE)
IMPLEMENTATION
6.5
I
Q
6.6
TXI
LPF-1
6.11
TXQ
LPF-1
6.8
6.7
T-LPF-2
6.12
6.13
Q-LPF-2
LO
6.10
90°
6.9
6.15
6.16
6.18
LIN/
NLIN
6.17
6.18

FIG. 6A

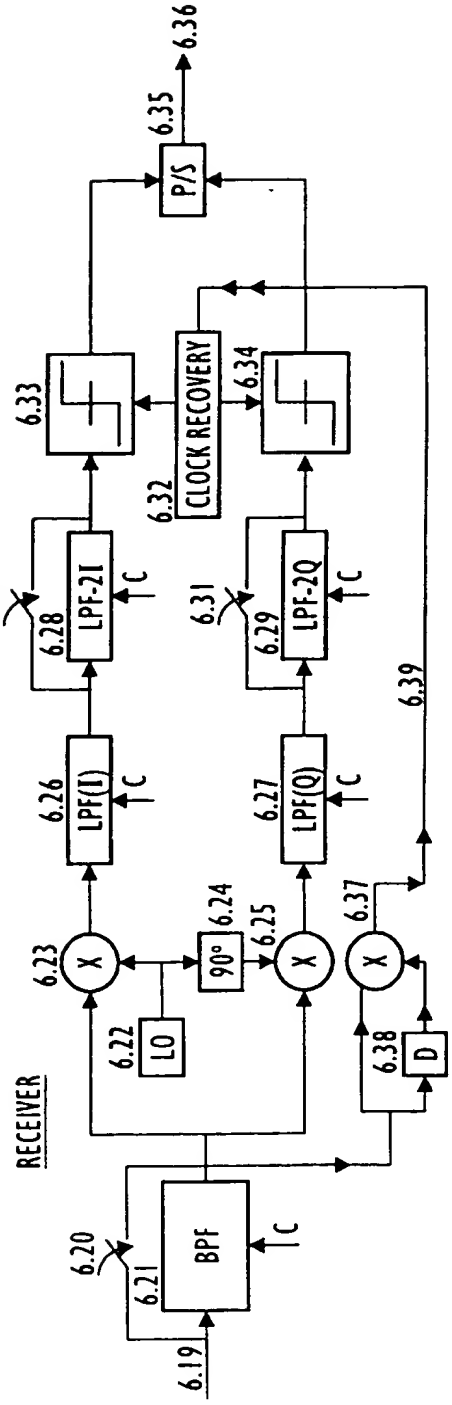

RECEIVER
6.19
6.20
6.21
BPF
6.22
LO
6.23
90°
6.24
6.25
6.37
6.38
D
6.26
LPF(I)
6.27
LPF(Q)
6.39
6.30
6.28
LPF-2I
6.31
6.29
LPF-2Q
6.32
CLOCK RECOVERY
6.33
6.34
6.35
P/S
6.36

FIG. 6B

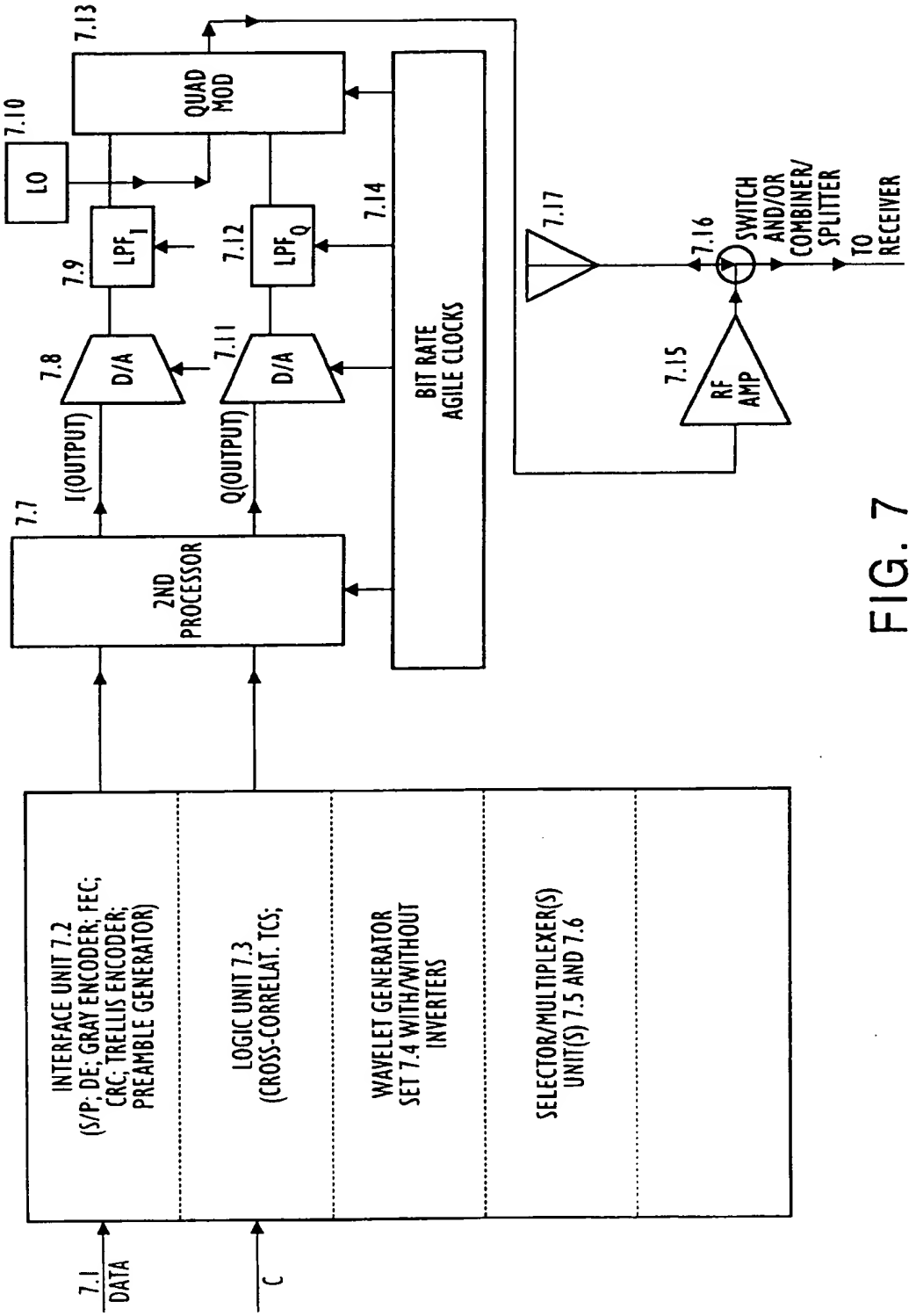

7.1
DATA
C
INTERFACE UNIT 7.2
(S/P; DE; GRAY ENCODER; FEC;
CRC; TRELLIS ENCODER;
PREAMBLE GENERATOR)
LOGIC UNIT 7.3
(CROSS-CORRELAT. TCS;
WAVELET GENERATOR
SET 7.4 WITH/WITHOUT
INVERTERS
SELECTOR/MULTIPLEXER(S)
UNIT(S) 7.5 AND 7.6
7.7
2ND
PROCESSOR
I(OUTPUT)
Q(OUTPUT)
7.8
D/A
7.11
D/A
7.9
LPF$_I$
7.12
LPF$_Q$
7.10
LO
7.13
QUAD
MOD
7.14
BIT RATE
AGILE CLOCKS
7.15
RF
AMP
7.16
SWITCH
AND/OR
COMBINER/
SPLITTER
7.17
TO
RECEIVER

FIG. 7

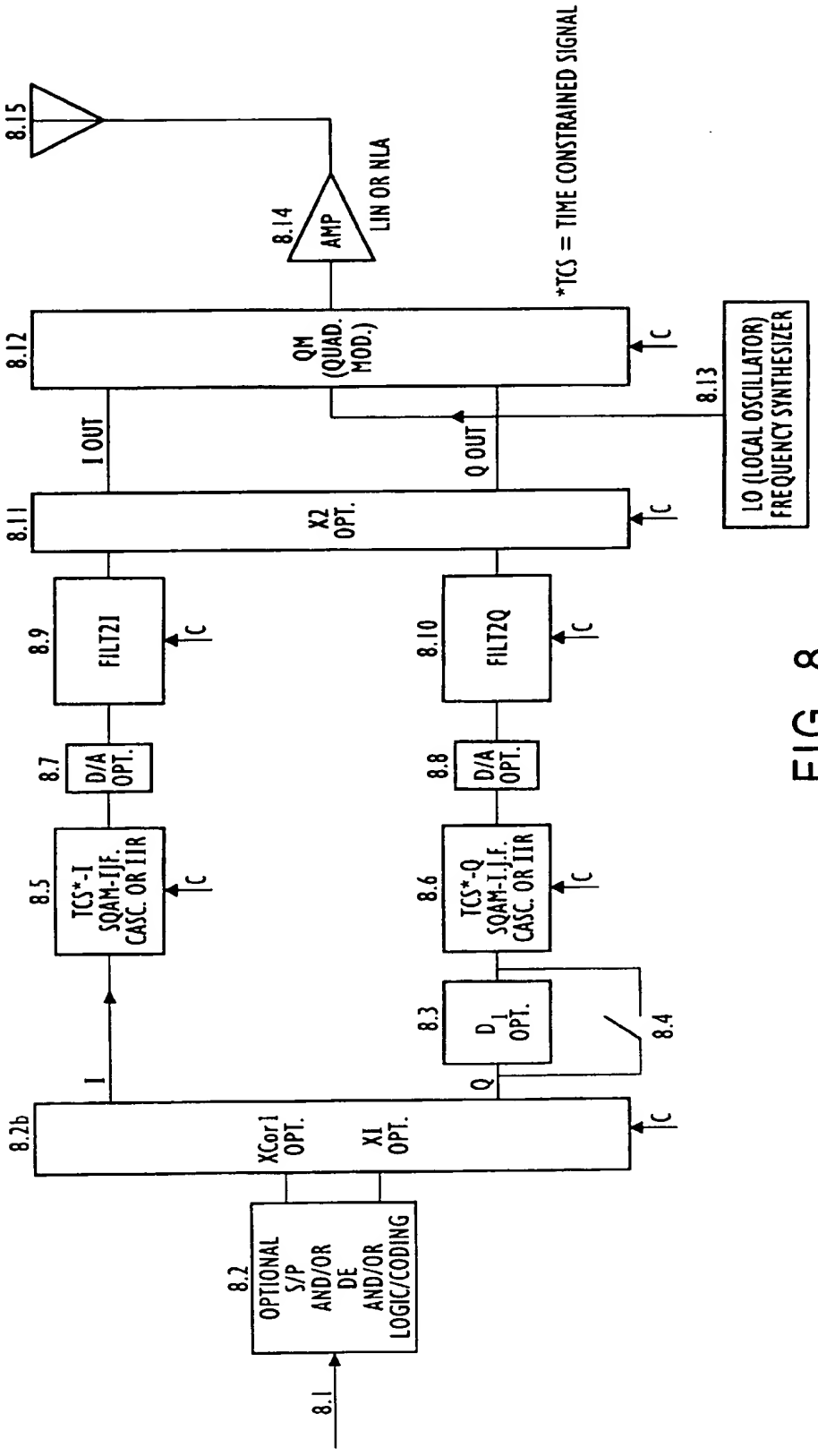

8.15
8.14
AMP
LIN OR NLA
*TCS = TIME CONSTRAINED SIGNAL
8.12
QM (QUAD. MOD.)
C
8.13
LO (LOCAL OSCILLATOR) FREQUENCY SYNTHESIZER
I OUT
Q OUT
8.11
X2 OPT.
C
8.9
FILT2I
C
8.10
FILT2Q
C
8.7
D/A OPT.
8.8
D/A OPT.
8.5
TCS*-I SQAM-IJF. CASC. OR IIR
C
8.6
TCS*-Q SQAM-I.J.F. CASC. OR IIR
C
8.3
D1 OPT.
8.4
I
Q
8.2b
XCor1 OPT.
XI OPT.
C
8.2
OPTIONAL S/P AND/OR DE AND/OR LOGIC/CODING
8.1

FIG. 8

FIG. 9A

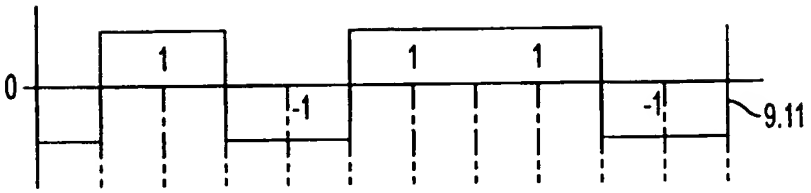


FIG. 9B

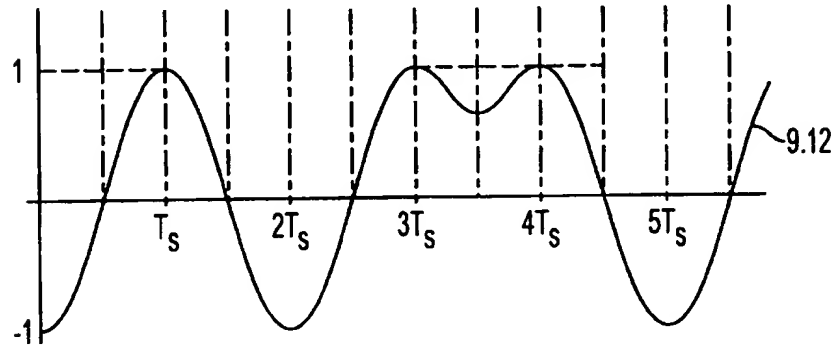


FIG. 9C

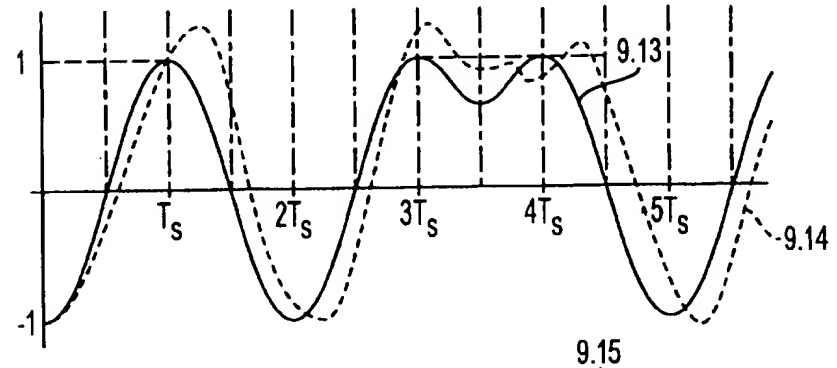
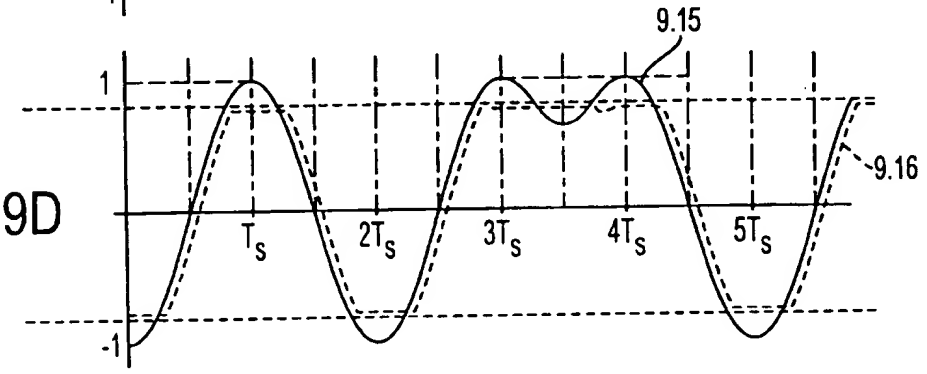


FIG. 9D



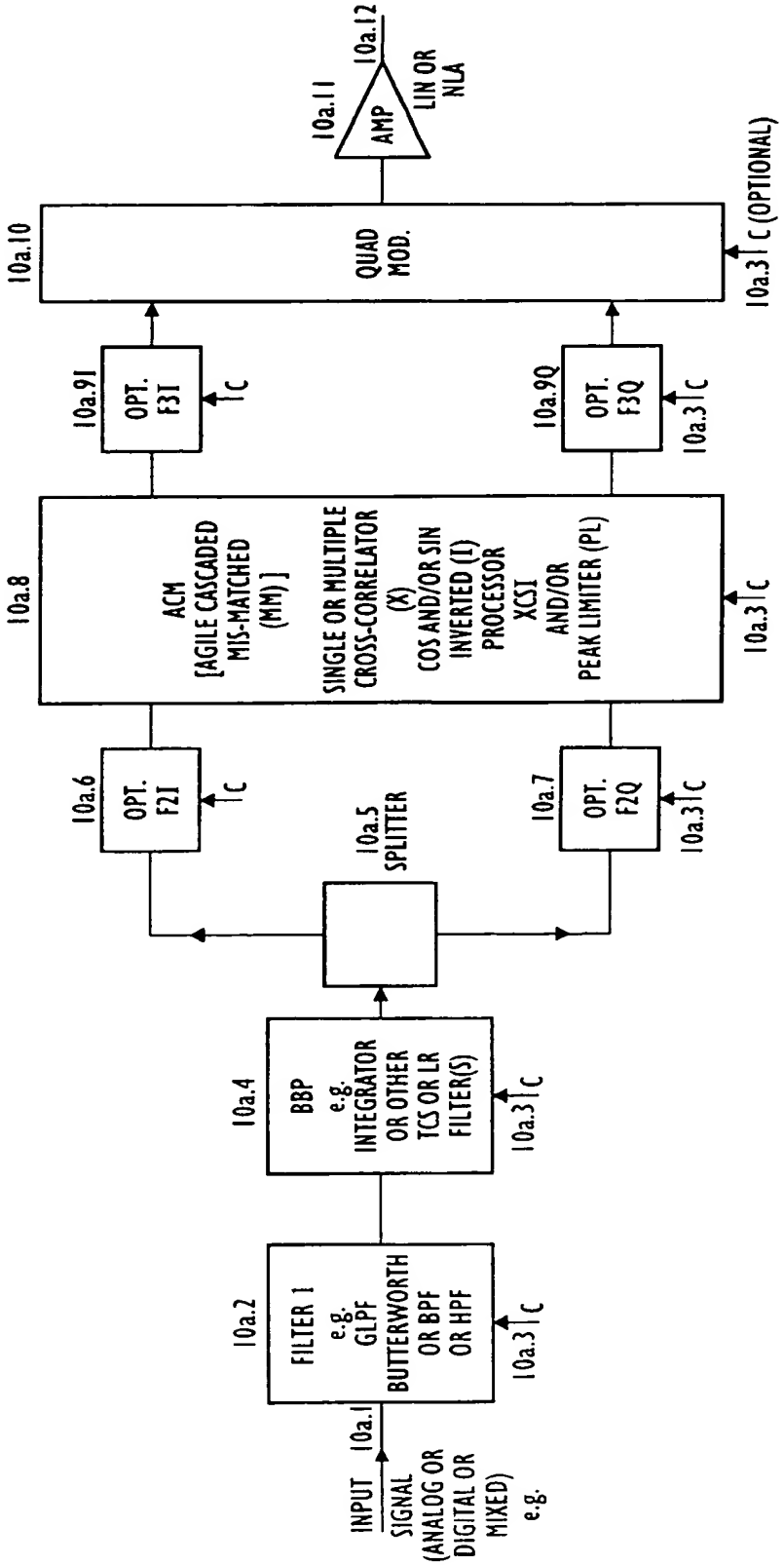

INPUT SIGNAL (ANALOG OR DIGITAL OR MIXED) e.g.
10a.1
10a.2
FILTER 1 e.g. GLPF BUTTERWORTH OR BPF OR HPF
10a.3 C
10a.4
BBP e.g. INTEGRATOR OR OTHER TCS OR LR FILTER(S)
10a.3 C
10a.5
SPLITTER
10a.6
OPT. F2I
C
10a.7
OPT. F2Q
10a.3 C
10a.8
ACM [AGILE CASCADED MIS-MATCHED (MM)] SINGLE OR MULTIPLE CROSS-CORRELATOR (X) COS AND/OR SIN INVERTED (I) PROCESSOR XCSI AND/OR PEAK LIMITER (PL)
10a.3 C
10a.91
OPT. F3I
C
10a.9Q
OPT. F3Q
10a.3 C
10a.10
QUAD MOD.
10a.3 C (OPTIONAL)
10a.11
AMP
10a.12
LIN OR NLA

FIG. 10A

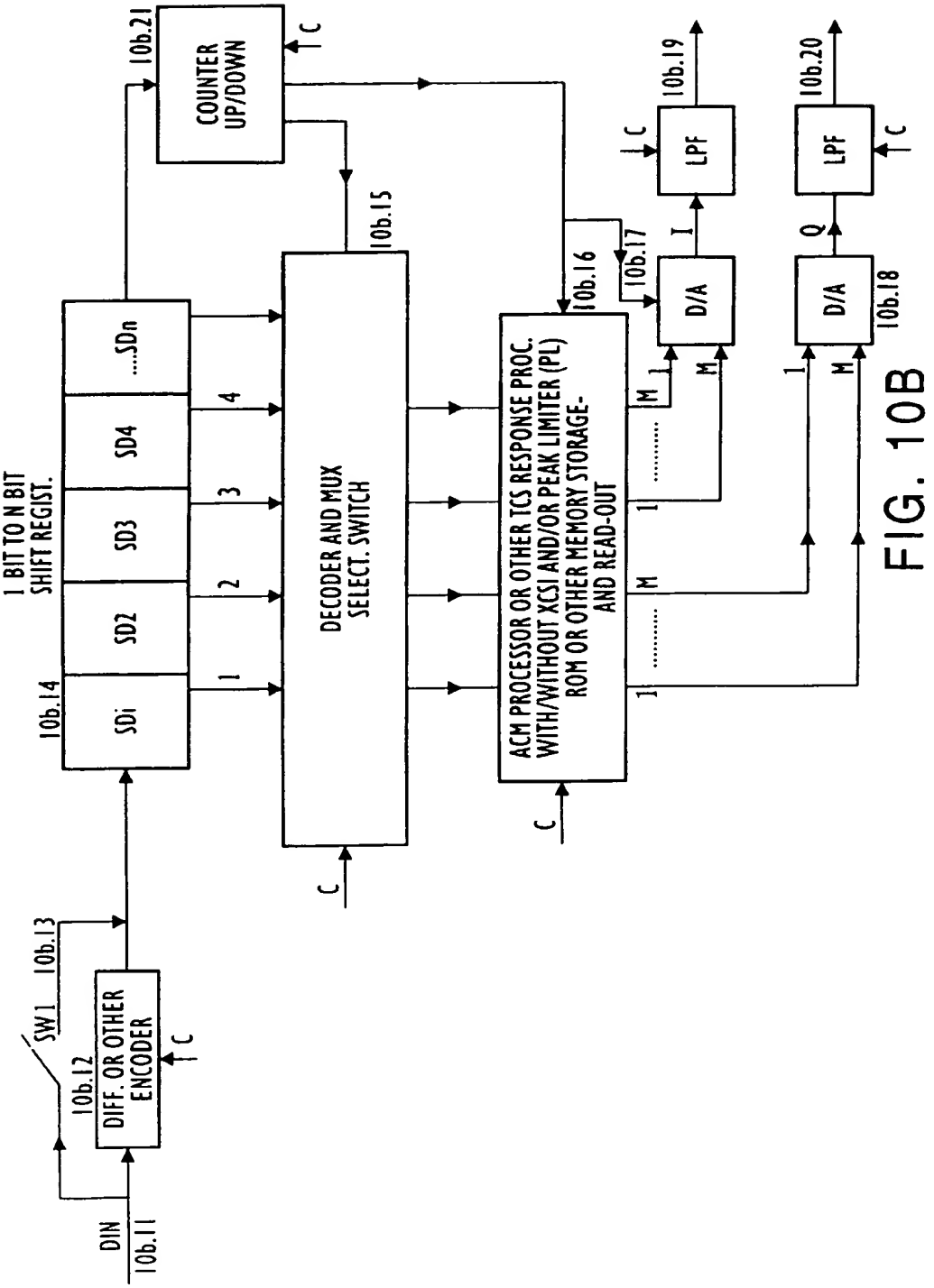

10b.21
COUNTER UP/DOWN
C
10b.15
DECODER AND MUX SELECT. SWITCH
1 BIT TO N BIT SHIFT REGIST.
10b.14
SDi
SD2
SD3
SD4
....SDn
1
2
3
4
ACM PROCESSOR OR OTHER TCS RESPONSE PROC. WITH/WITHOUT XCSI AND/OR PEAK LIMITER (PL) ROM OR OTHER MEMORY STORAGE- AND READ-OUT
10b.16
10b.17
D/A
I
Q
LPF
10b.19
10b.20
10b.18
M
1
SW1
10b.13
10b.12
DIFF. OR OTHER ENCODER
DIN
10b.11

FIG. 10B

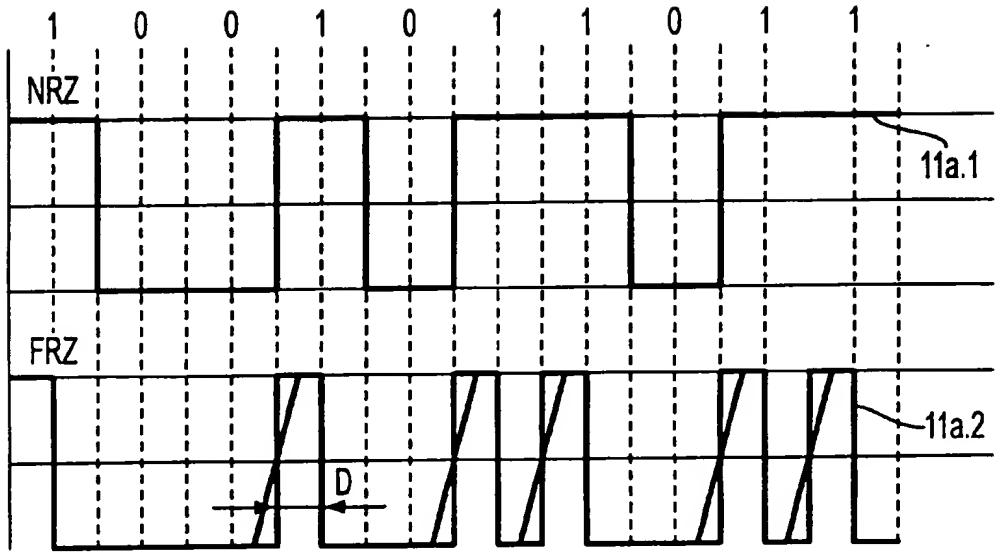
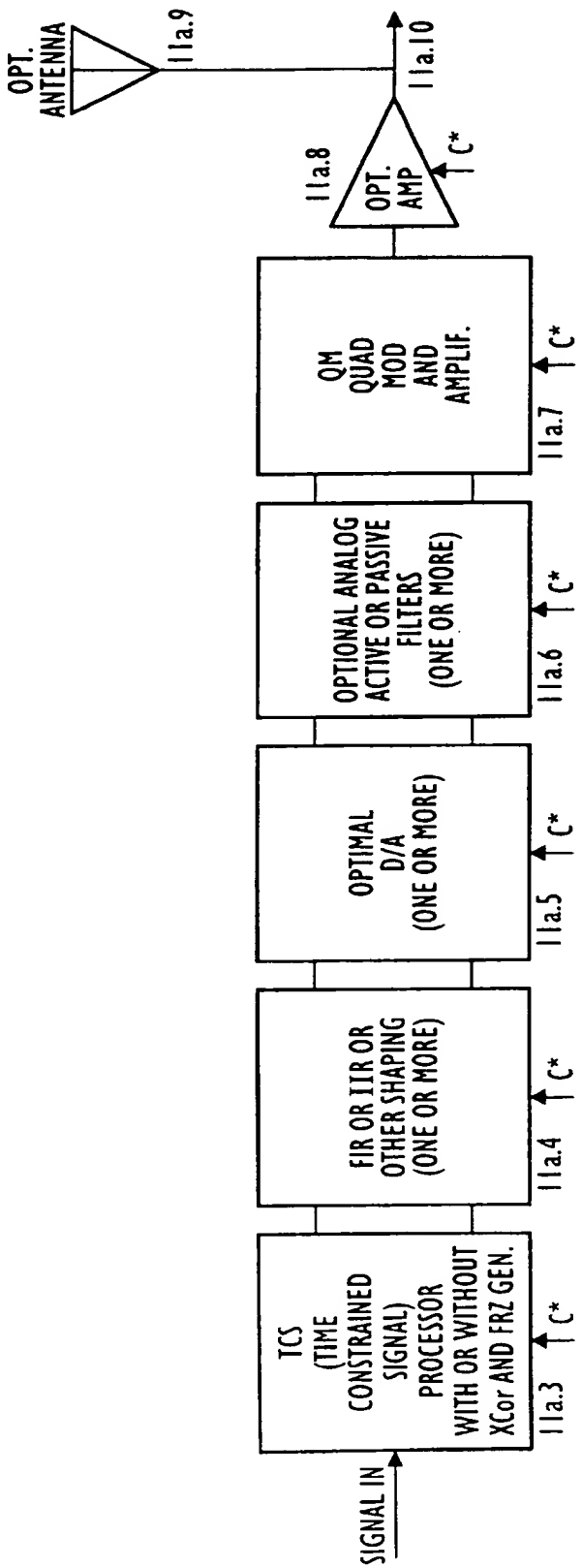


FIG. 11A



C* DESIGNATES OPTIONAL CLOCK AND/OR CONTROL SIGNAL

FIG. 11B

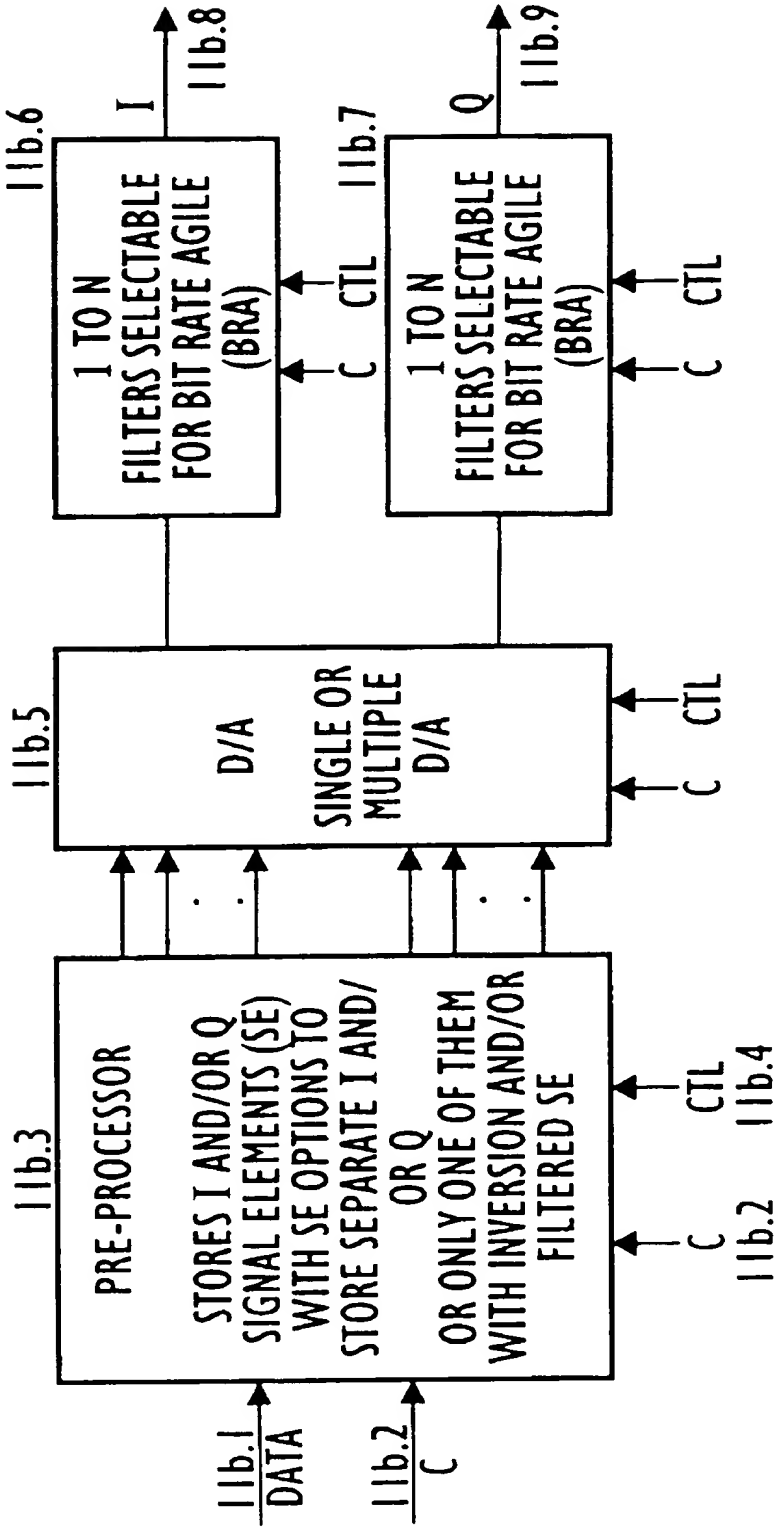

11b.1
DATA
11b.2
C
11b.3
PRE-PROCESSOR
STORES I AND/OR Q SIGNAL ELEMENTS (SE) WITH SE OPTIONS TO STORE SEPARATE I AND/OR Q OR ONLY ONE OF THEM WITH INVERSION AND/OR FILTERED SE
C CTL
11b.4
11b.5
D/A
SINGLE OR MULTIPLE D/A
C CTL
11b.6
1 TO N FILTERS SELECTABLE FOR BIT RATE AGILE (BRA)
C CTL
I
11b.8
11b.7
1 TO N FILTERS SELECTABLE FOR BIT RATE AGILE (BRA)
C CTL
Q
11b.9

FIG. 11C

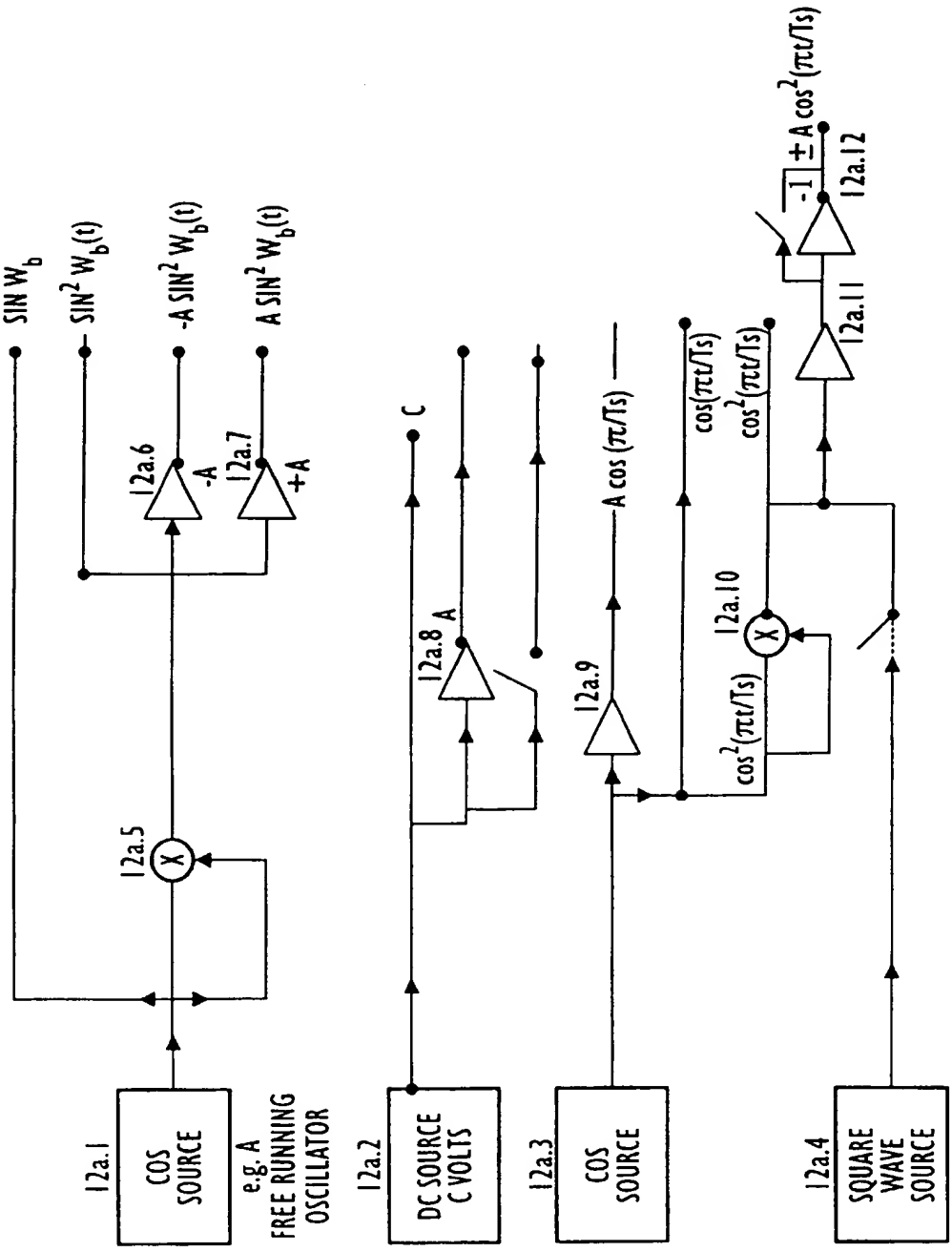

SIN W_b
SIN^2 W_b(t)
-A SIN^2 W_b(t)
A SIN^2 W_b(t)
12a.6
-A
12a.7
+A
12a.5
12a.1
COS SOURCE
e.g. A FREE RUNNING OSCILLATOR
C
12a.8
A
12a.2
DC SOURCE C VOLTS
A cos (πt/Ts)
12a.9
12a.3
COS SOURCE
cos(πt/Ts)
cos^2(πt/Ts)
12a.10
cos^2(πt/Ts)
12a.11
-1
$\pm$ A cos^2(πt/Ts)
12a.12
12a.4
SQUARE WAVE SOURCE

FIG. 12A

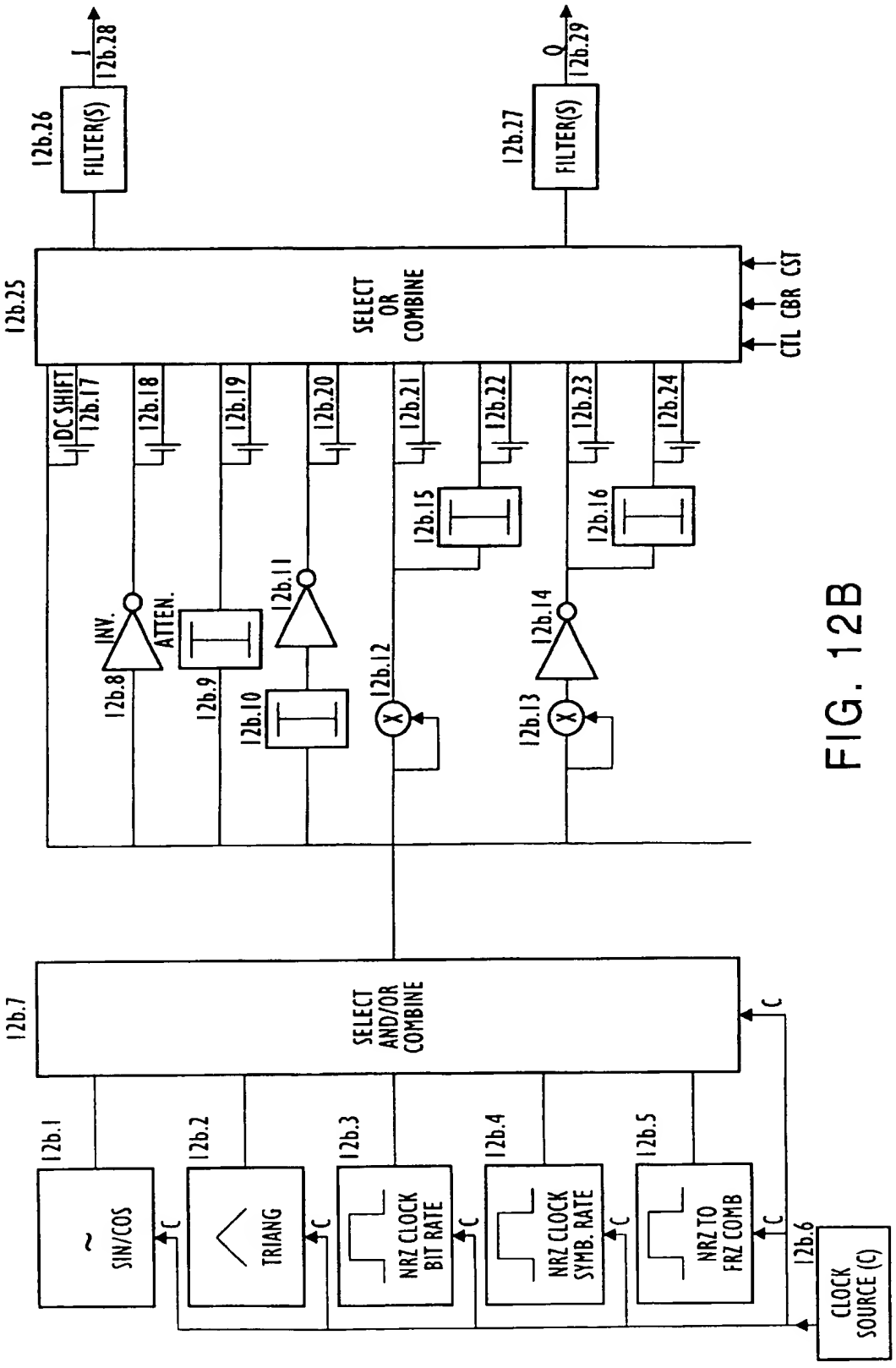

12b.1
SIN/COS
12b.2
TRIANG
12b.3
NRZ CLOCK BIT RATE
12b.4
NRZ CLOCK SYMB. RATE
12b.5
NRZ TO FRZ COMB
12b.6
CLOCK SOURCE (C)
12b.7
SELECT AND/OR COMBINE
C
12b.8
INV.
12b.9
ATTEN.
12b.10
12b.11
12b.12
12b.13
12b.14
12b.15
12b.16
12b.17
DC SHIFT
12b.18
12b.19
12b.20
12b.21
12b.22
12b.23
12b.24
12b.25
SELECT OR COMBINE
CTL CBR CST
12b.26
FILTER(S)
I
12b.28
12b.27
FILTER(S)
Q
12b.29

FIG. 12B

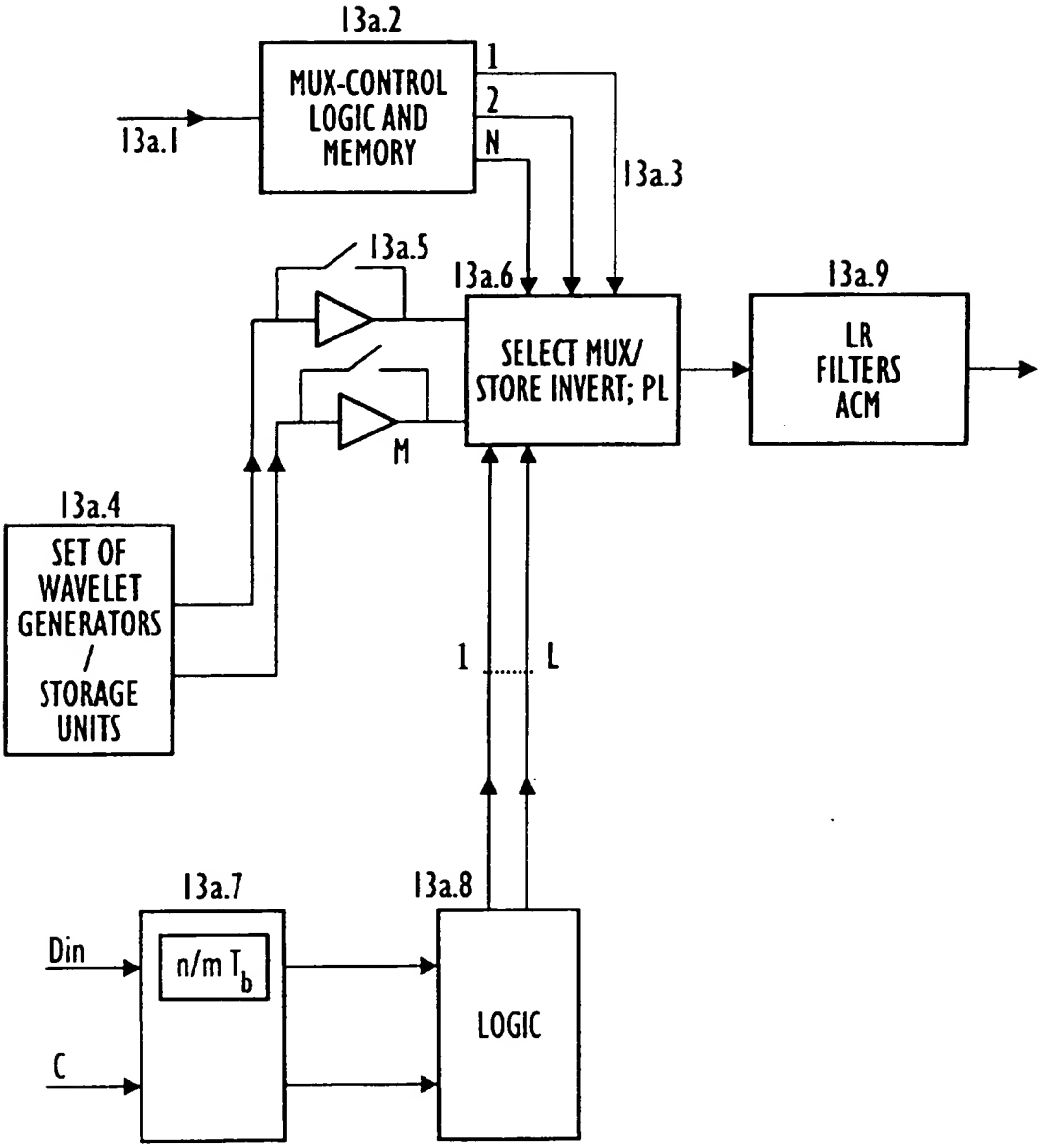

13a.2
MUX-CONTROL LOGIC AND MEMORY
1
2
N
13a.1
13a.3
13a.5
13a.6
13a.9
SELECT MUX/ STORE INVERT; PL
LR FILTERS ACM
M
13a.4
SET OF WAVELET GENERATORS / STORAGE UNITS
1 L
13a.7
13a.8
Din
n/m T_b
C
LOGIC

FIG. 13A

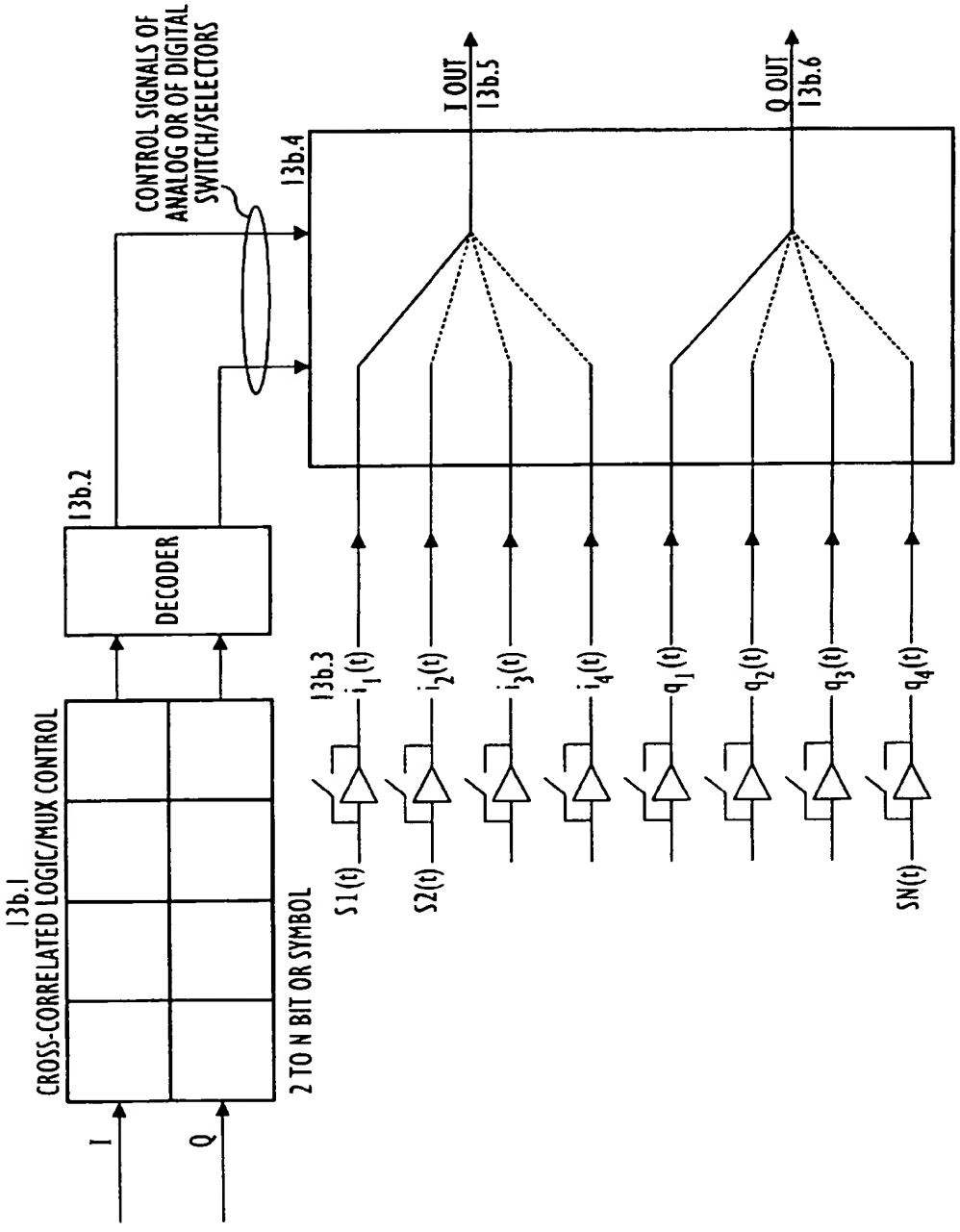

CONTROL SIGNALS OF ANALOG OR OF DIGITAL SWITCH/SELECTORS
13b.4
I OUT
13b.5
Q OUT
13b.6
13b.2
DECODER
13b.3
$i_1(t)$
$i_2(t)$
$i_3(t)$
$i_4(t)$
$q_1(t)$
$q_2(t)$
$q_3(t)$
$q_4(t)$
S1(t)
S2(t)
SN(t)
13b.1
CROSS-CORRELATED LOGIC/MUX CONTROL
2 TO N BIT OR SYMBOL
I
Q

FIG. 13B

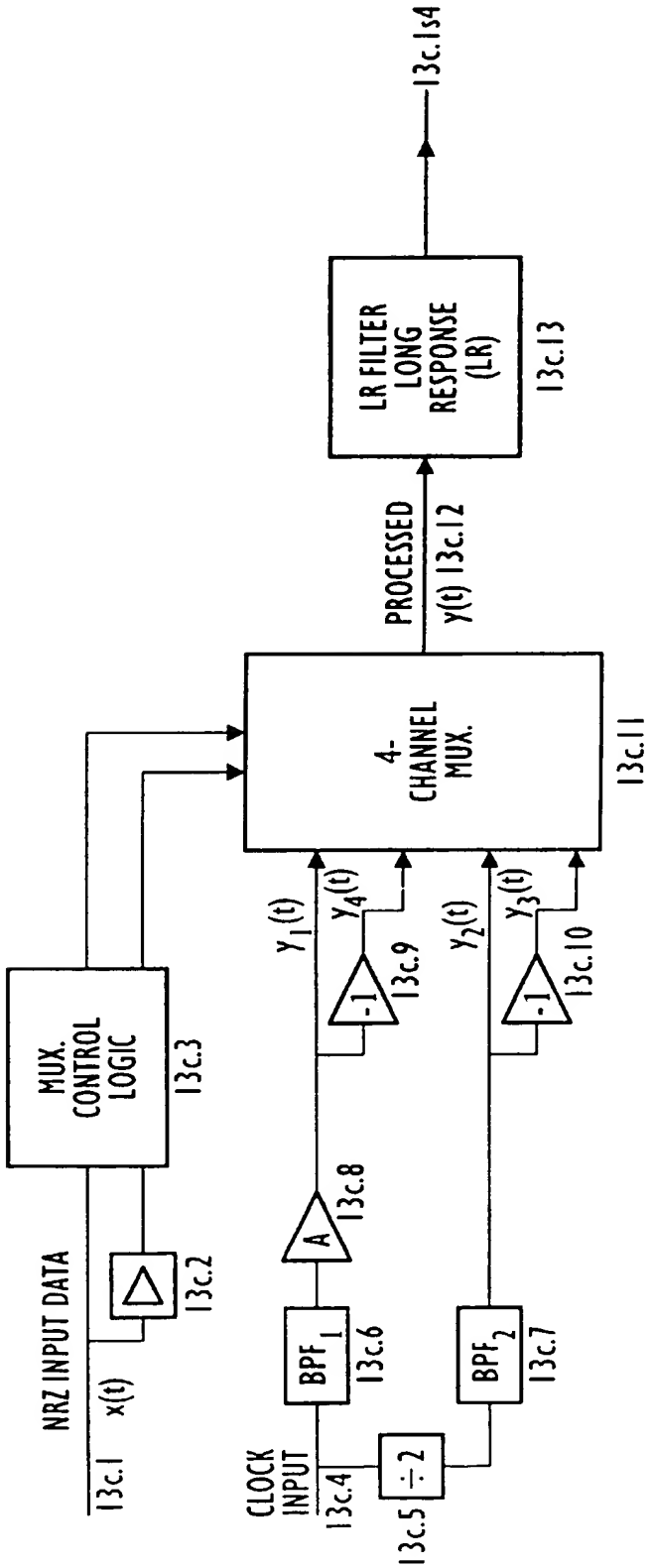

13c.1s4
LR FILTER LONG RESPONSE (LR)
13c.13
PROCESSED y(t) 13c.12
4-CHANNEL MUX.
13c.11
MUX. CONTROL LOGIC
13c.3
NRZ INPUT DATA
x(t)
13c.1
13c.2
A
13c.8
BPF1
13c.6
BPF2
13c.7
CLOCK INPUT
13c.4
÷2
13c.5
-1
13c.9
-1
13c.10
y1(t)
y4(t)
y2(t)
y3(t)

FIG. 13C

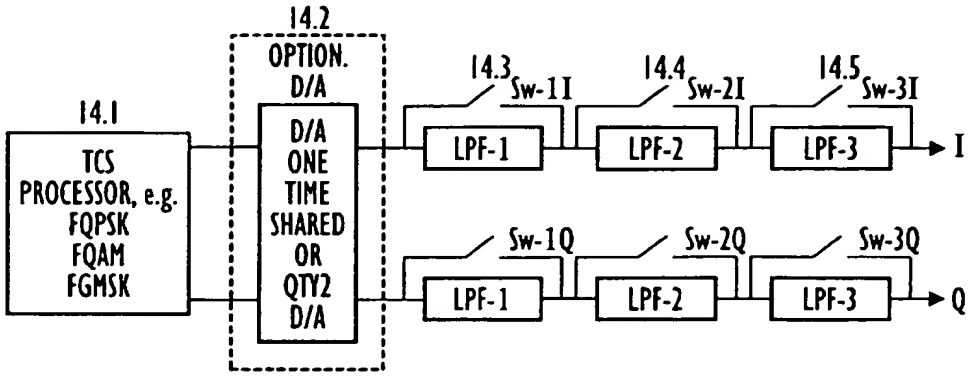


FIG. 14A

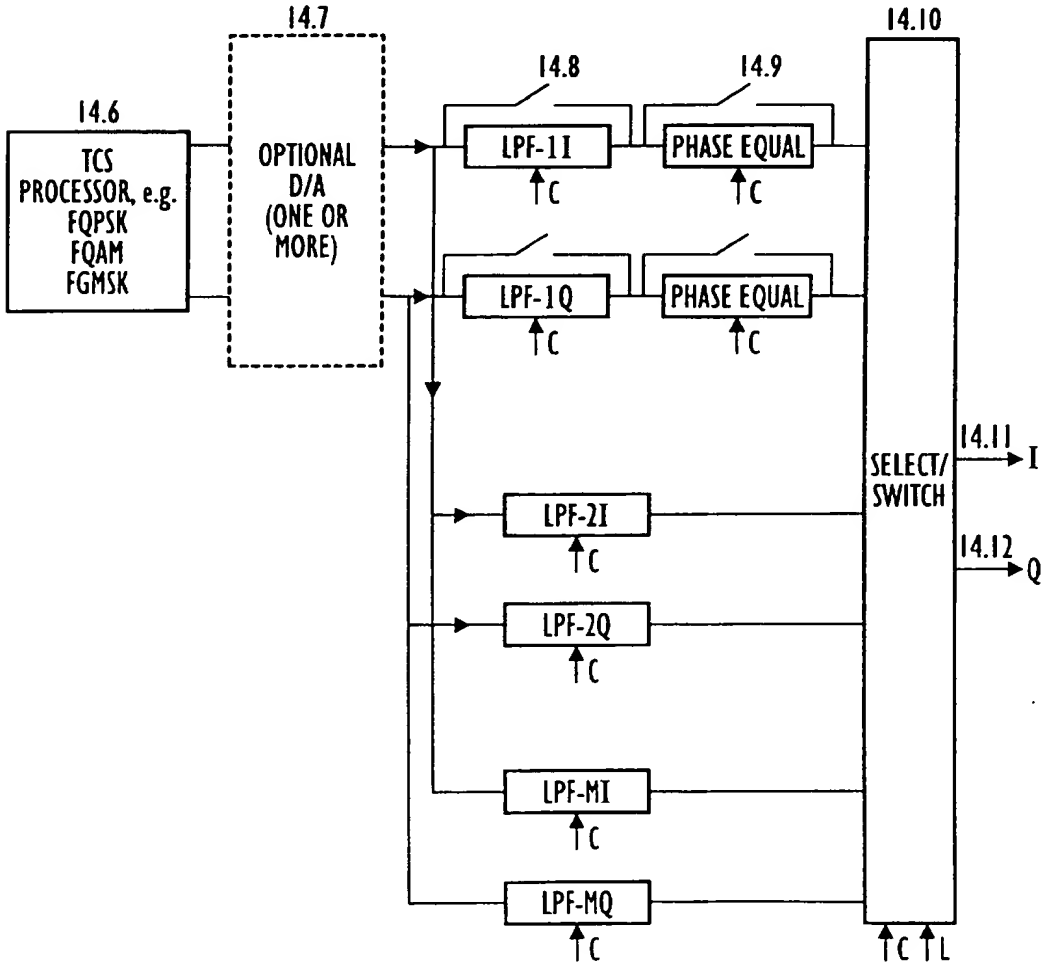


FIG. 14B

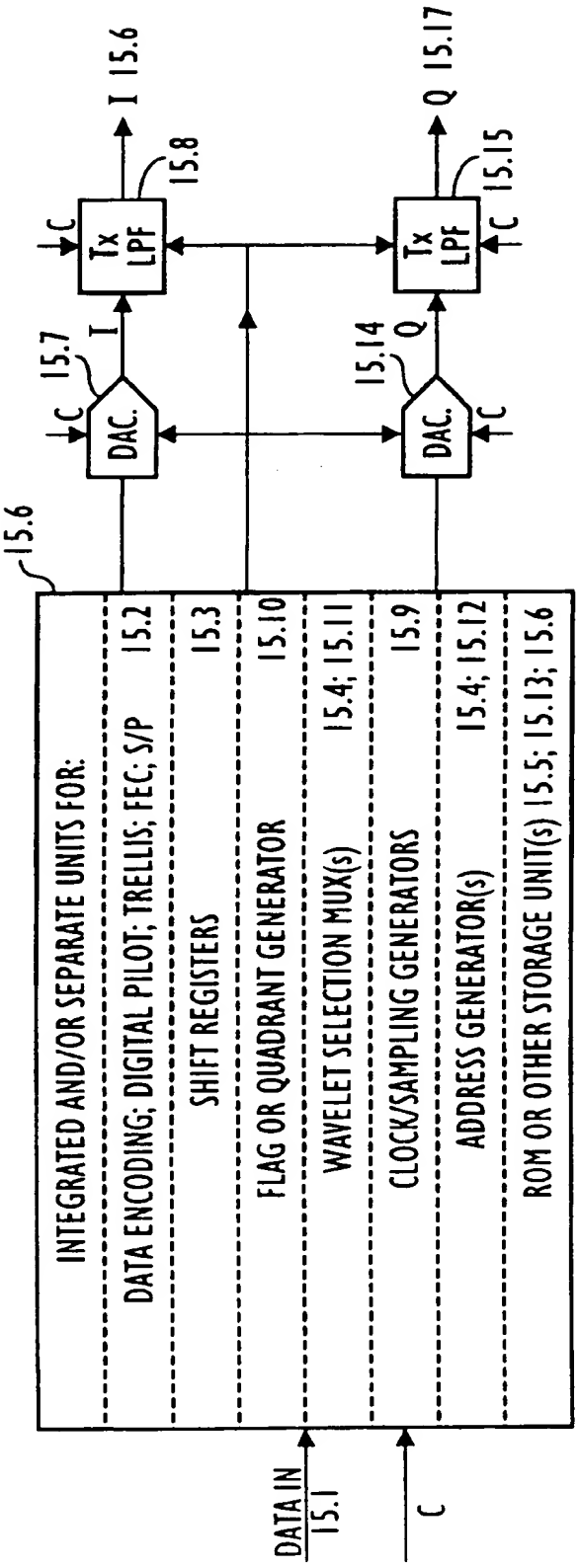

I 15.6
Q 15.17
15.8
15.15
C
Tx LPF
Tx LPF
C
15.7
I
15.14
Q
C
DAC.
DAC.
C
15.6
INTEGRATED AND/OR SEPARATE UNITS FOR:
DATA ENCODING; DIGITAL PILOT; TRELLIS; FEC; S/P 15.2
SHIFT REGISTERS 15.3
FLAG OR QUADRANT GENERATOR 15.10
WAVELET SELECTION MUX(s) 15.4; 15.11
CLOCK/SAMPLING GENERATORS 15.9
ADDRESS GENERATOR(s) 15.4; 15.12
ROM OR OTHER STORAGE UNIT(s) 15.5; 15.13; 15.6
DATA IN 15.1
C

FIG. 15

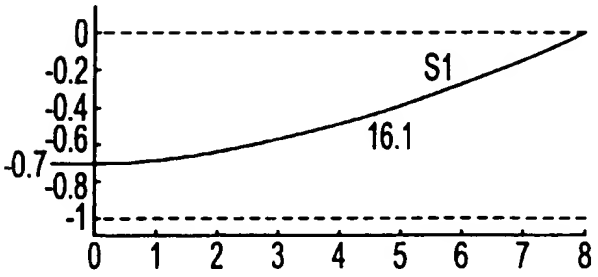


FIG. 16A

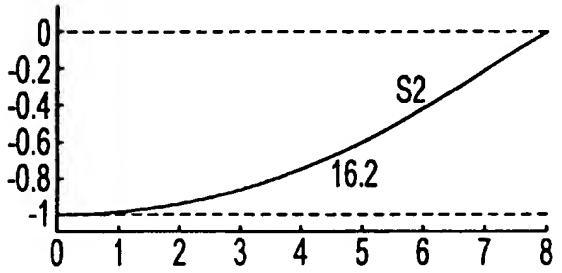


FIG. 16B

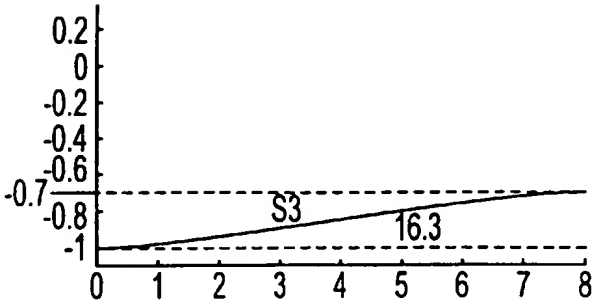


FIG. 16C

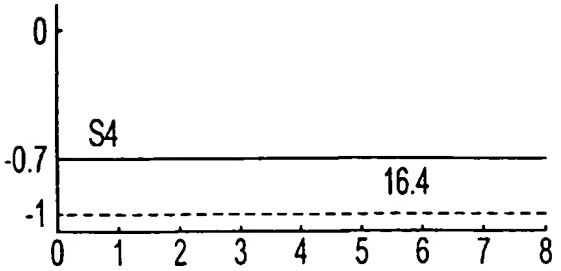


FIG. 16D

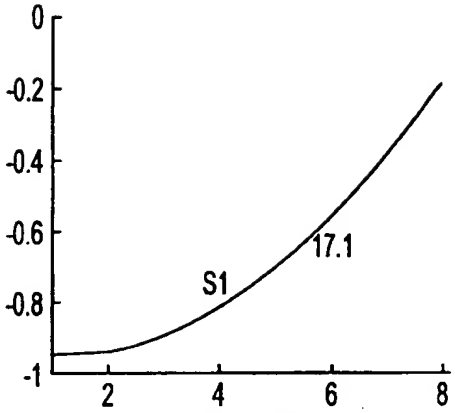


FIG. 17A

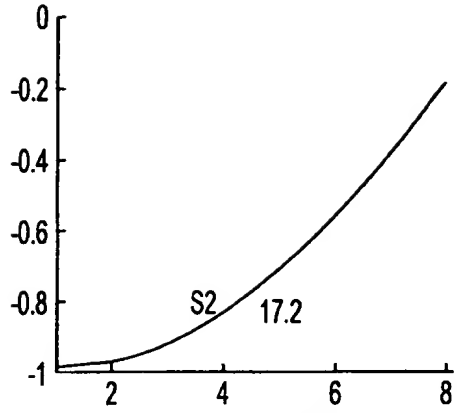


FIG. 17B

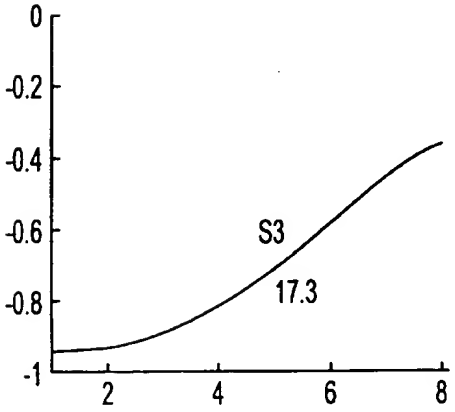


FIG. 17C

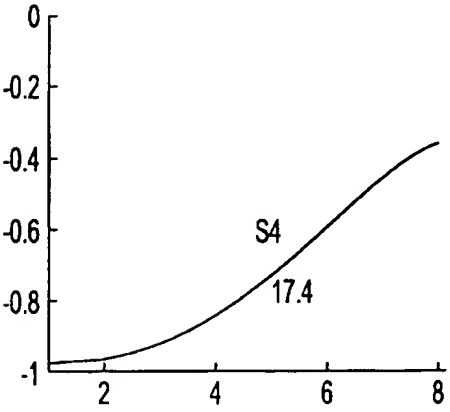


FIG. 17D

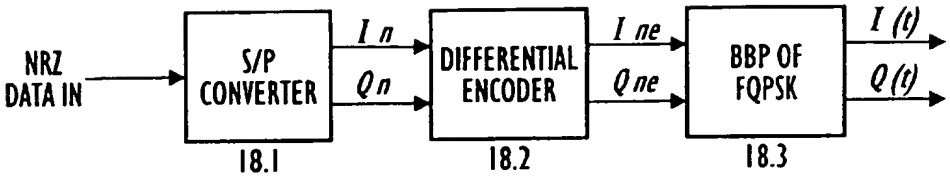


FIG. 18A

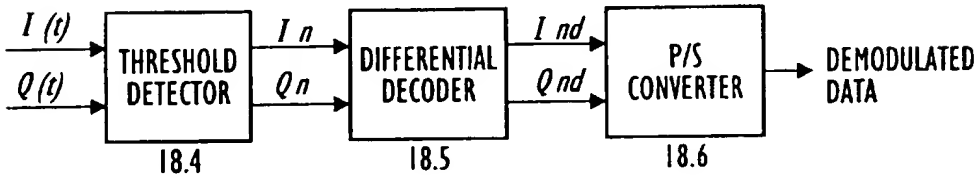
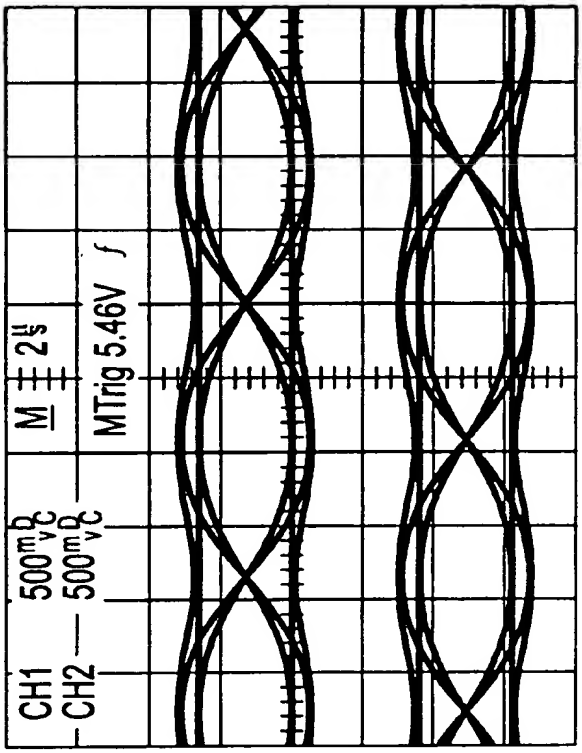
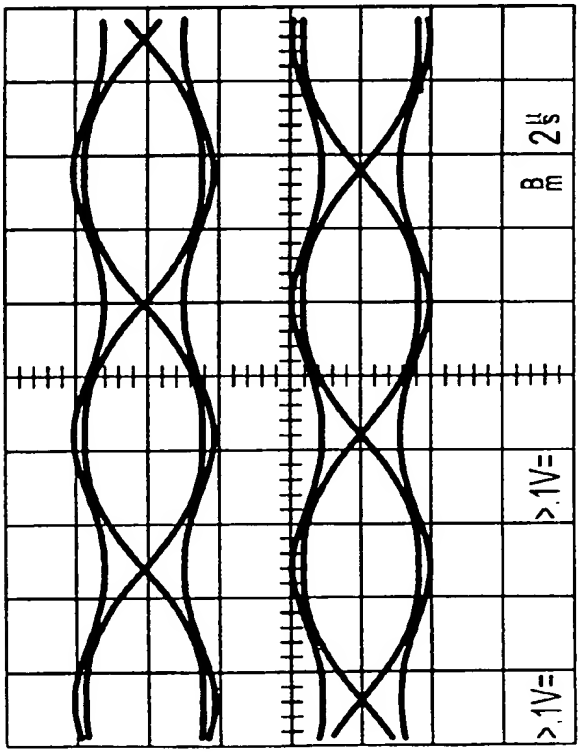


FIG. 18B



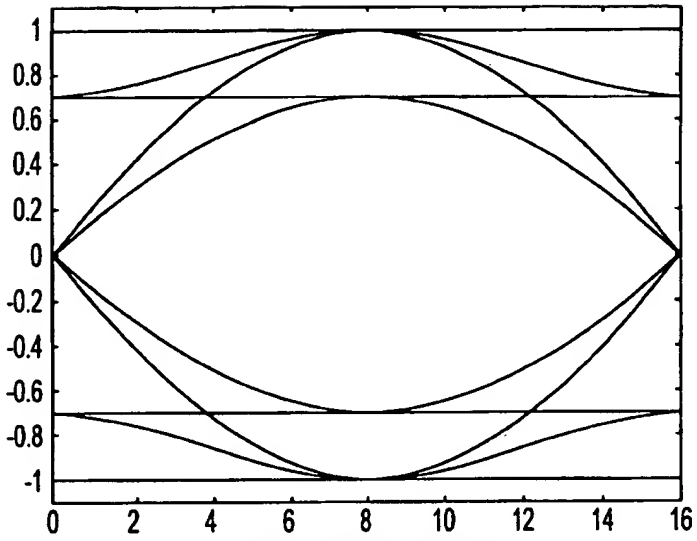
FQPSK MEAS. MIN. FILT. A=0.7

FIG. 19B



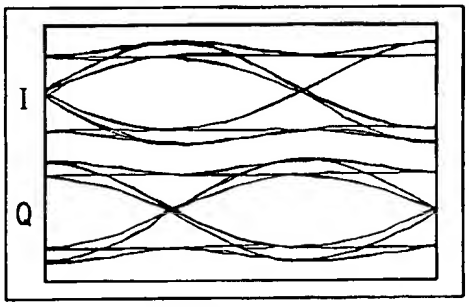
FGMSK (BTb=0.3)

FIG. 19A



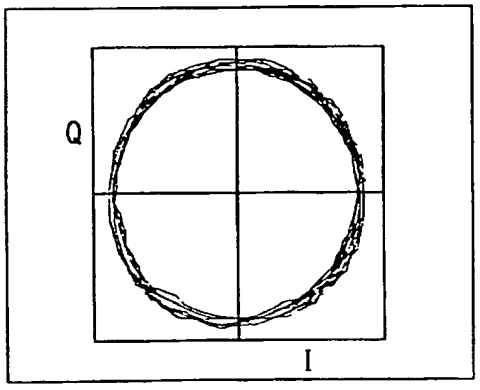
FQPSK COMPUTER. GENER.
A=0.7, NO POST TCS FILTERING

FIG. 19C



FQPSK-B MEAS.

FIG. 19D



FQPSK-B. VECTOR CONSTELLATION

FIG. 19E

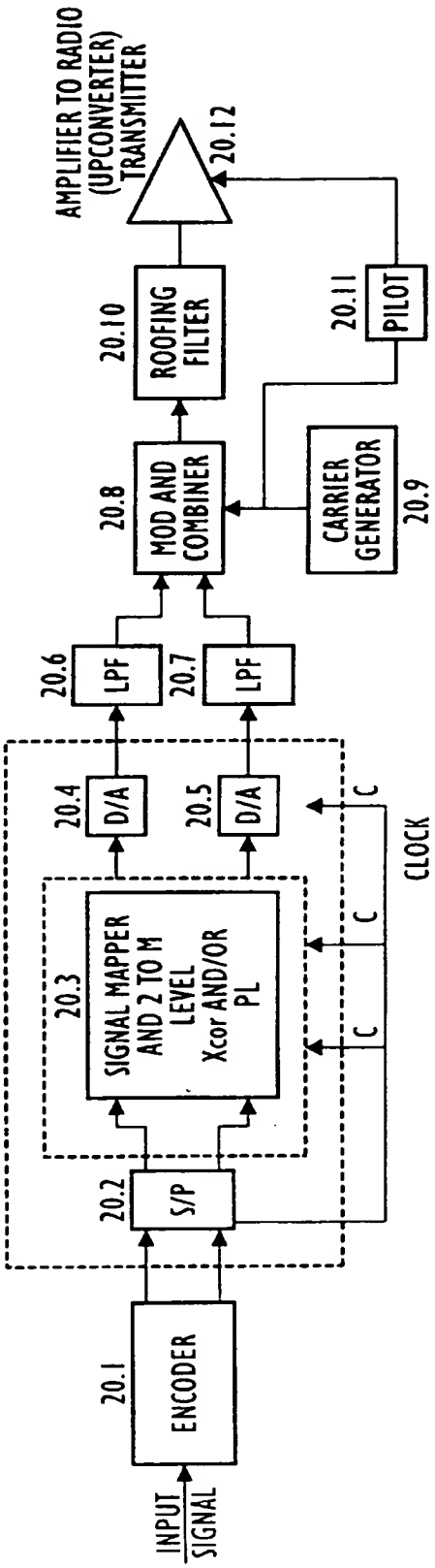

INPUT SIGNAL
20.1 ENCODER
20.2 S/P
20.3 SIGNAL MAPPER AND 2 TO M LEVEL Xcor AND/OR PL
20.4 D/A
20.5 D/A
20.6 LPF
20.7 LPF
20.8 MOD AND COMBINER
CARRIER GENERATOR 20.9
20.10 ROOFING FILTER
20.11 PILOT
AMPLIFIER TO RADIO (UPCONVERTER) TRANSMITTER 20.12
CLOCK
C
C
C

FIG. 20

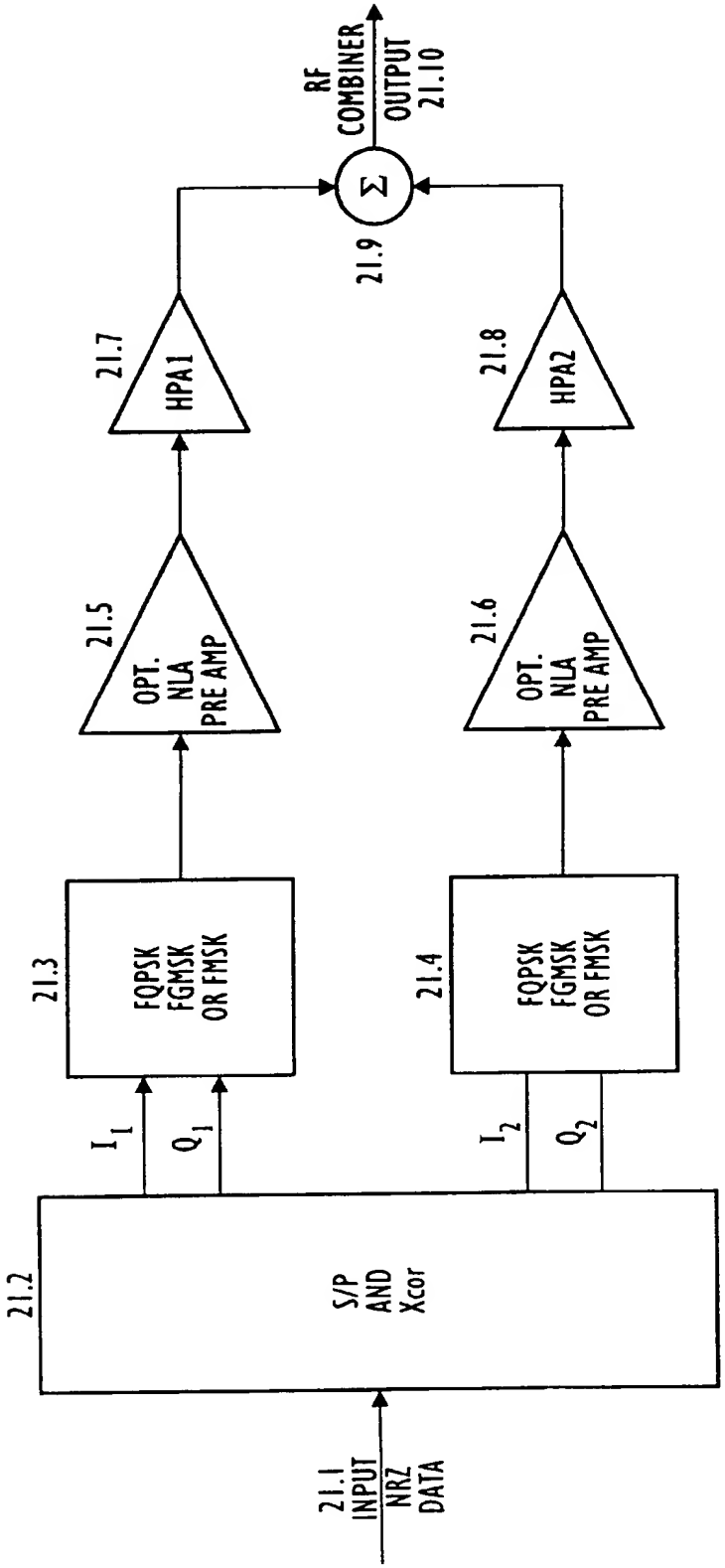

21.1
INPUT
NRZ
DATA
21.2
S/P
AND
Xcor
I_1
Q_1
I_2
Q_2
21.3
FQPSK
FGMSK
OR FMSK
21.4
FQPSK
FGMSK
OR FMSK
21.5
OPT.
NLA
PRE AMP
21.6
OPT.
NLA
PRE AMP
21.7
HPA1
21.8
HPA2
21.9
Σ
RF
COMBINER
OUTPUT
21.10

FIG. 21

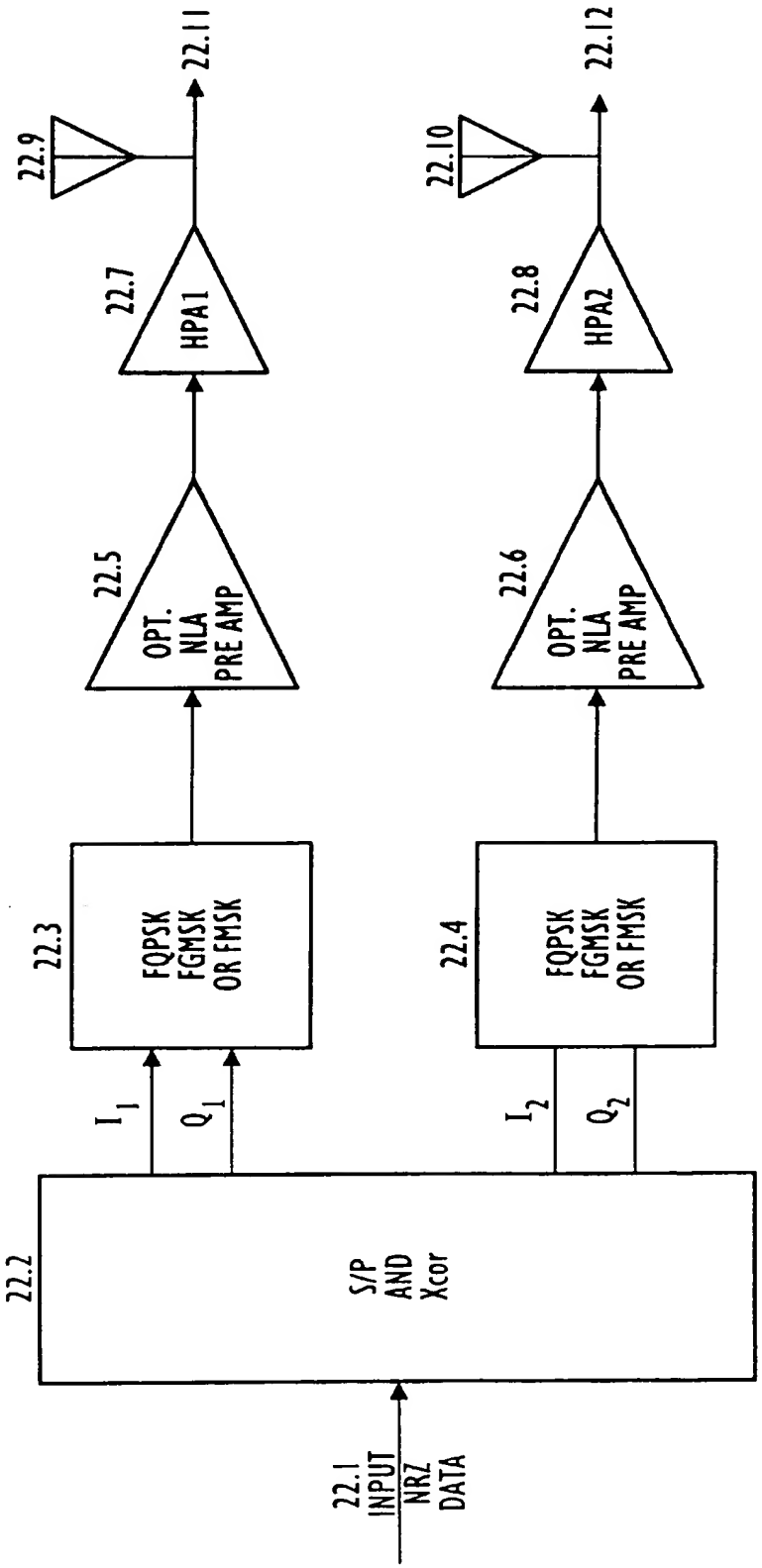

22.1
INPUT
NRZ
DATA
22.2
S/P
AND
Xcor
I_1
Q_1
I_2
Q_2
22.3
FQPSK
FGMSK
OR FMSK
22.4
FQPSK
FGMSK
OR FMSK
22.5
OPT.
NLA
PRE AMP
22.6
OPT.
NLA
PRE AMP
22.7
HPA1
22.8
HPA2
22.9
22.10
22.11
22.12

FIG. 22

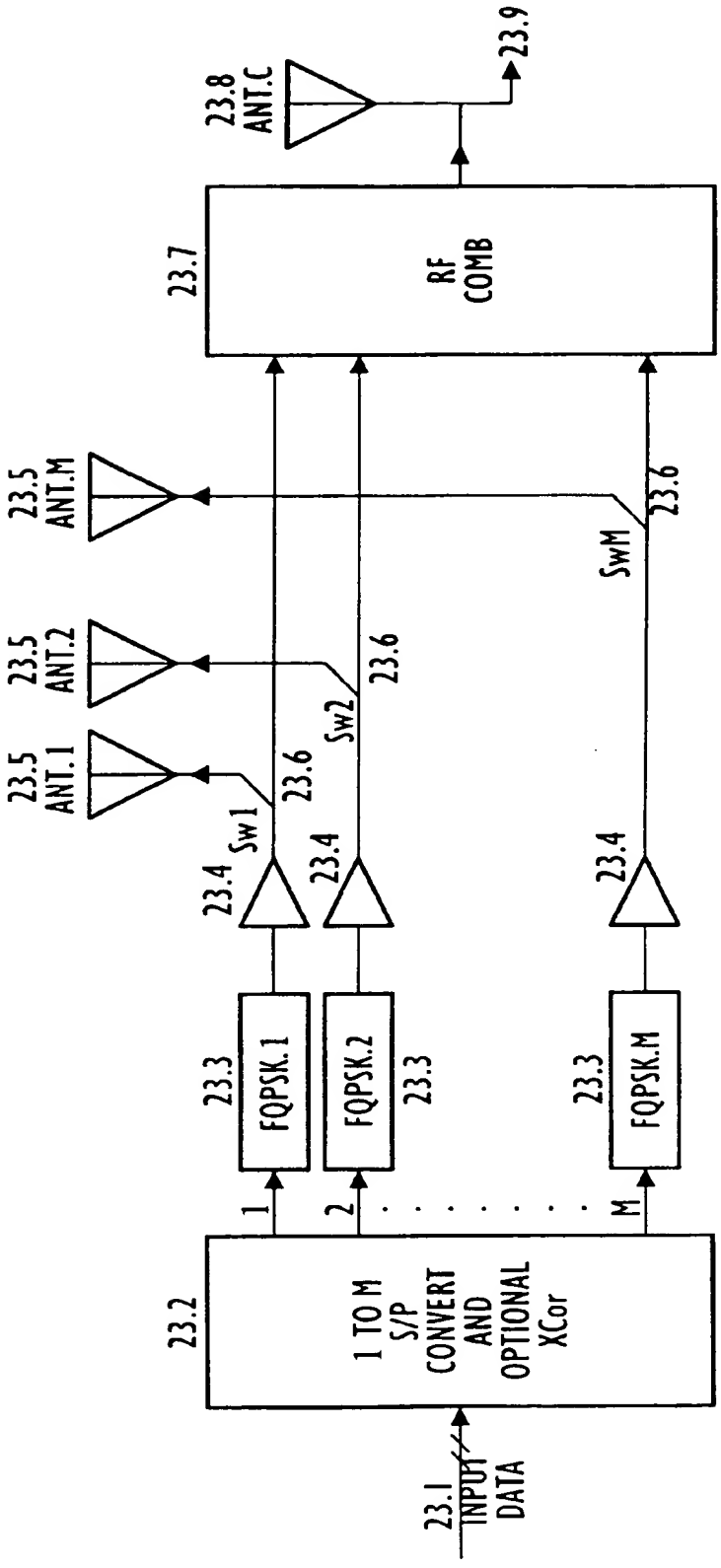

23.1
INPUT
DATA
23.2
1 TO M
S/P
CONVERT
AND
OPTIONAL
XCor
1
2
M
23.3
FQPSK.1
23.3
FQPSK.2
23.3
FQPSK.M
23.4
23.4
23.4
Sw1
Sw2
SwM
23.5
ANT.1
23.5
ANT.2
23.5
ANT.M
23.6
23.6
23.6
23.7
RF
COMB
23.8
ANT.C
23.9

FIG. 23

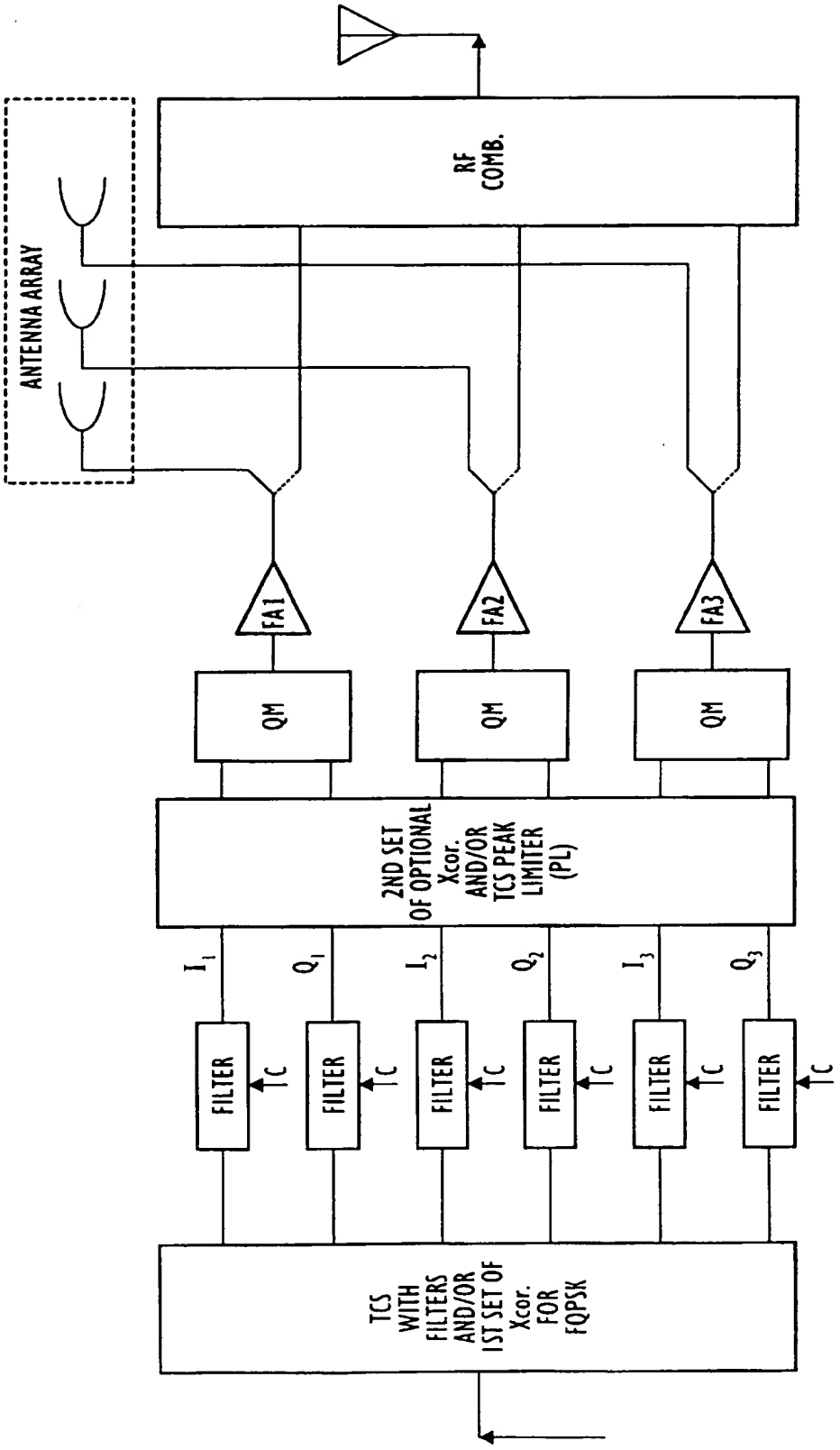

ANTENNA ARRAY
RF COMB.
FA1
FA2
FA3
QM
QM
QM
2ND SET OF OPTIONAL Xcor. AND/OR TCS PEAK LIMITER (PL)
I1
Q1
I2
Q2
I3
Q3
FILTER
FILTER
FILTER
FILTER
FILTER
FILTER
TC
TC
TC
TC
TC
TC
TCS WITH FILTERS AND/OR 1ST SET OF Xcor. FOR FQPSK

FIG. 24

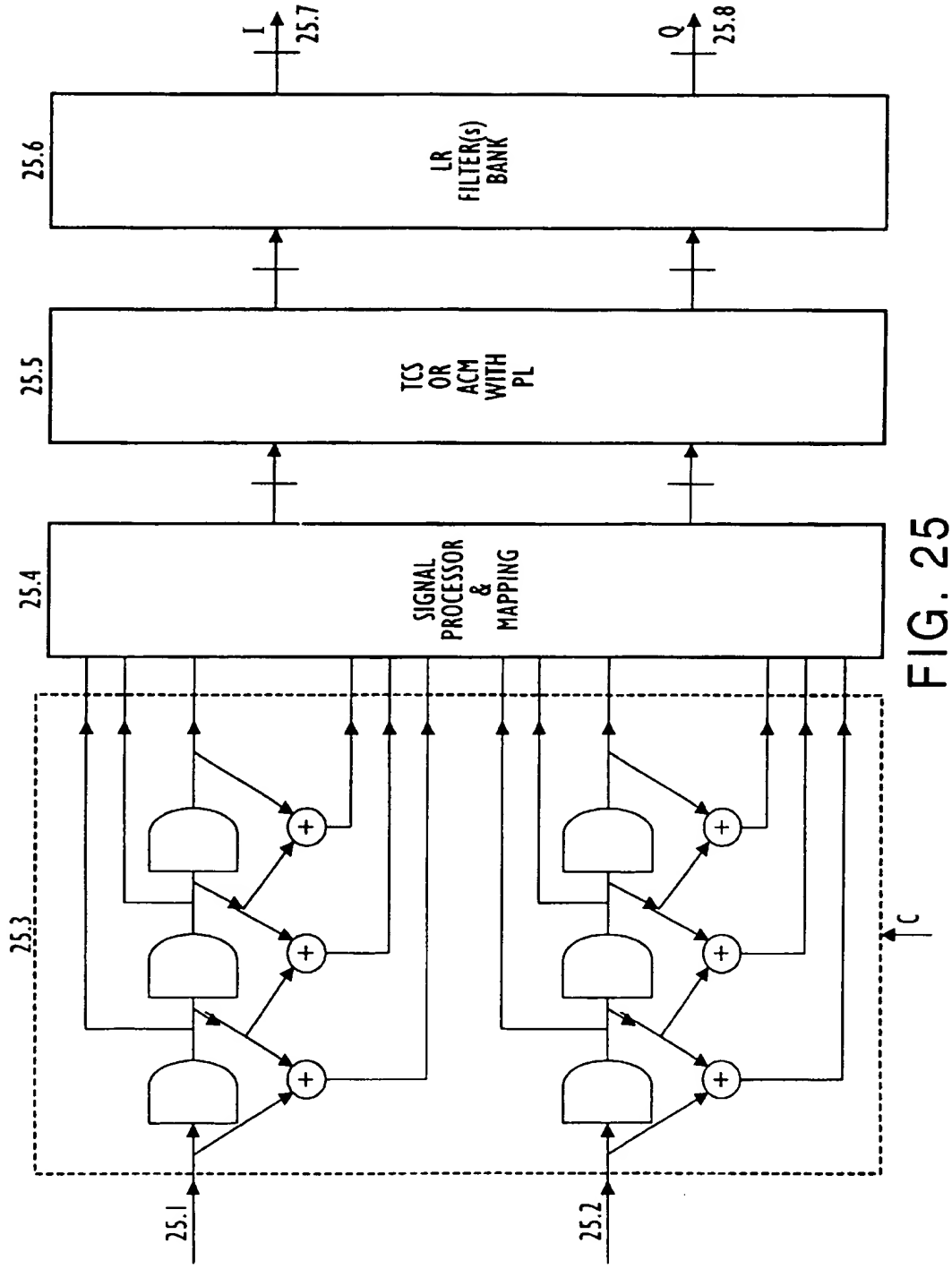

I
25.7
Q
25.8
25.6
LR FILTER(s) BANK
25.5
TCS OR ACM WITH PL
25.4
SIGNAL PROCESSOR & MAPPING
25.3
C
25.1
25.2

FIG. 25

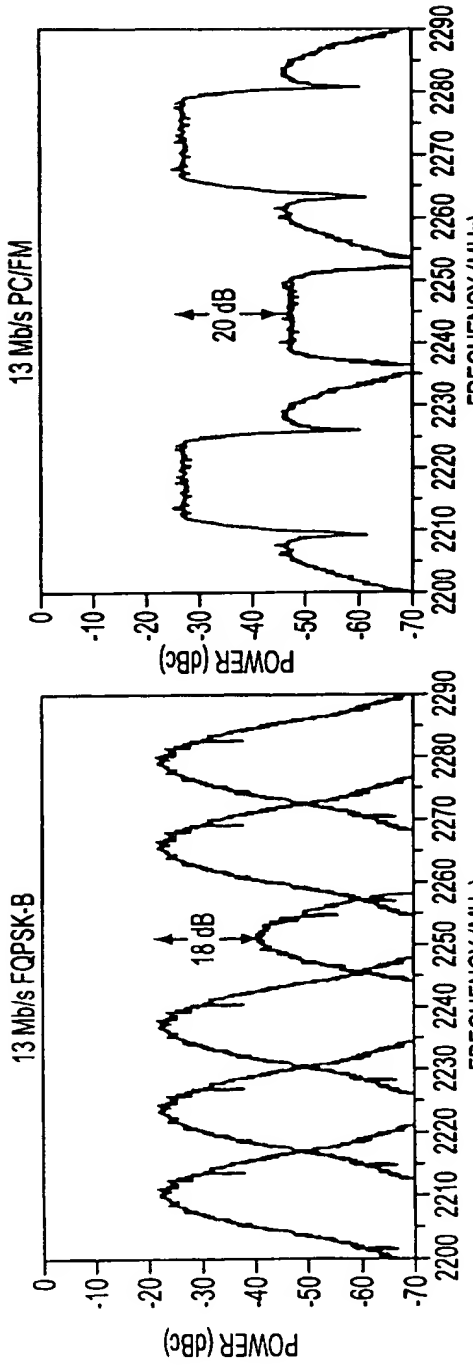


FIG. 26A

FIG. 26B

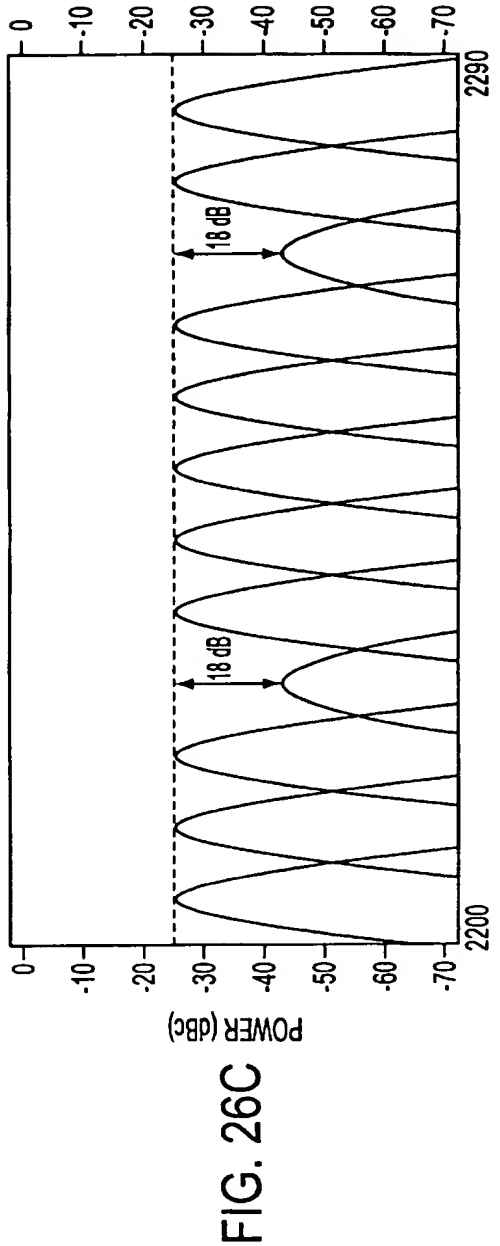


FIG. 26C

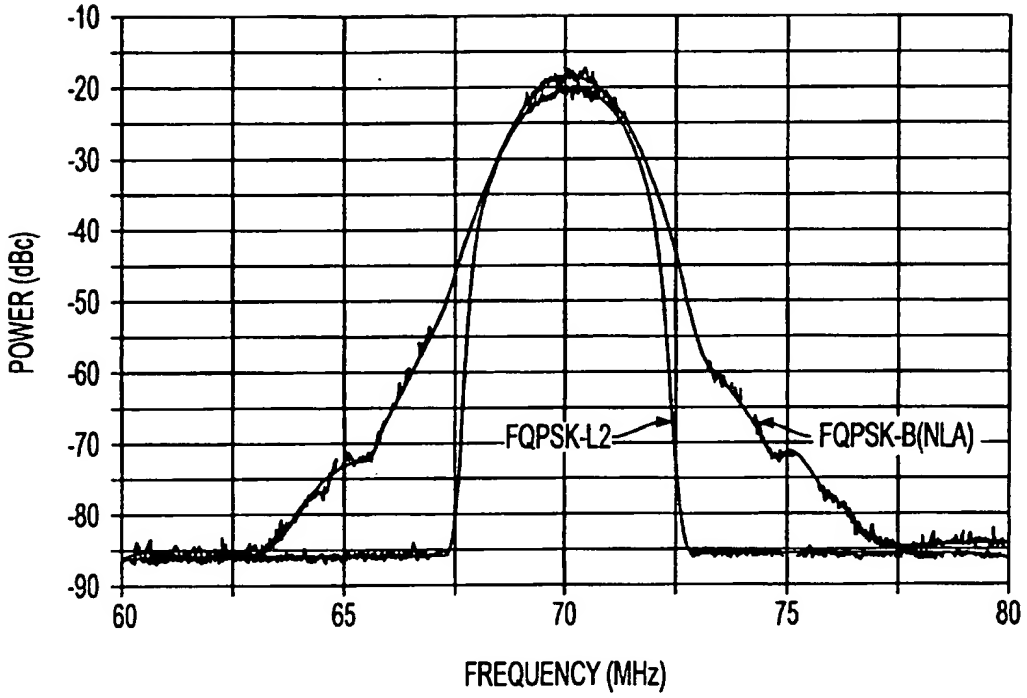


FIG. 27A

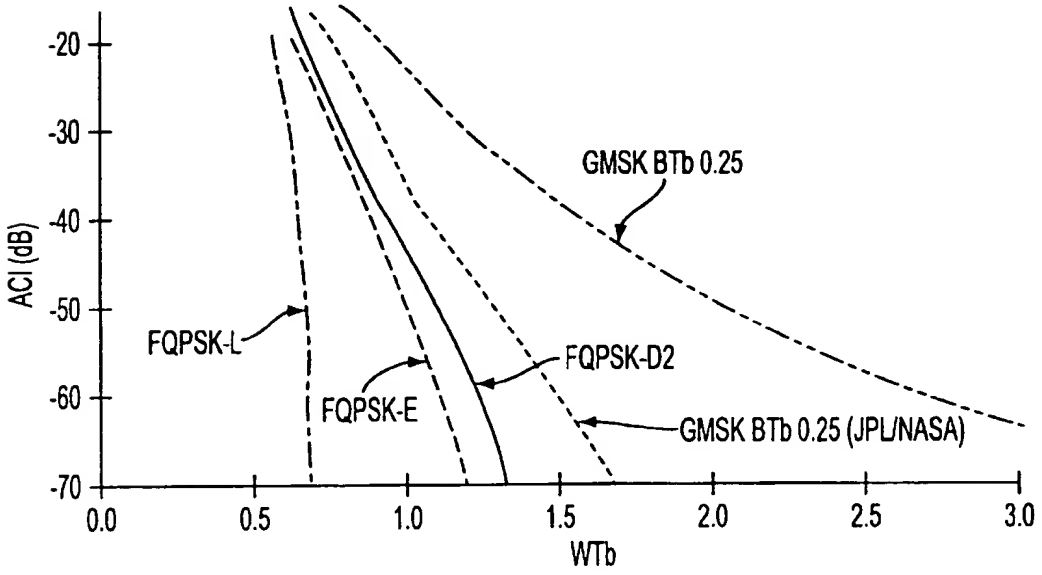


FIG. 27B

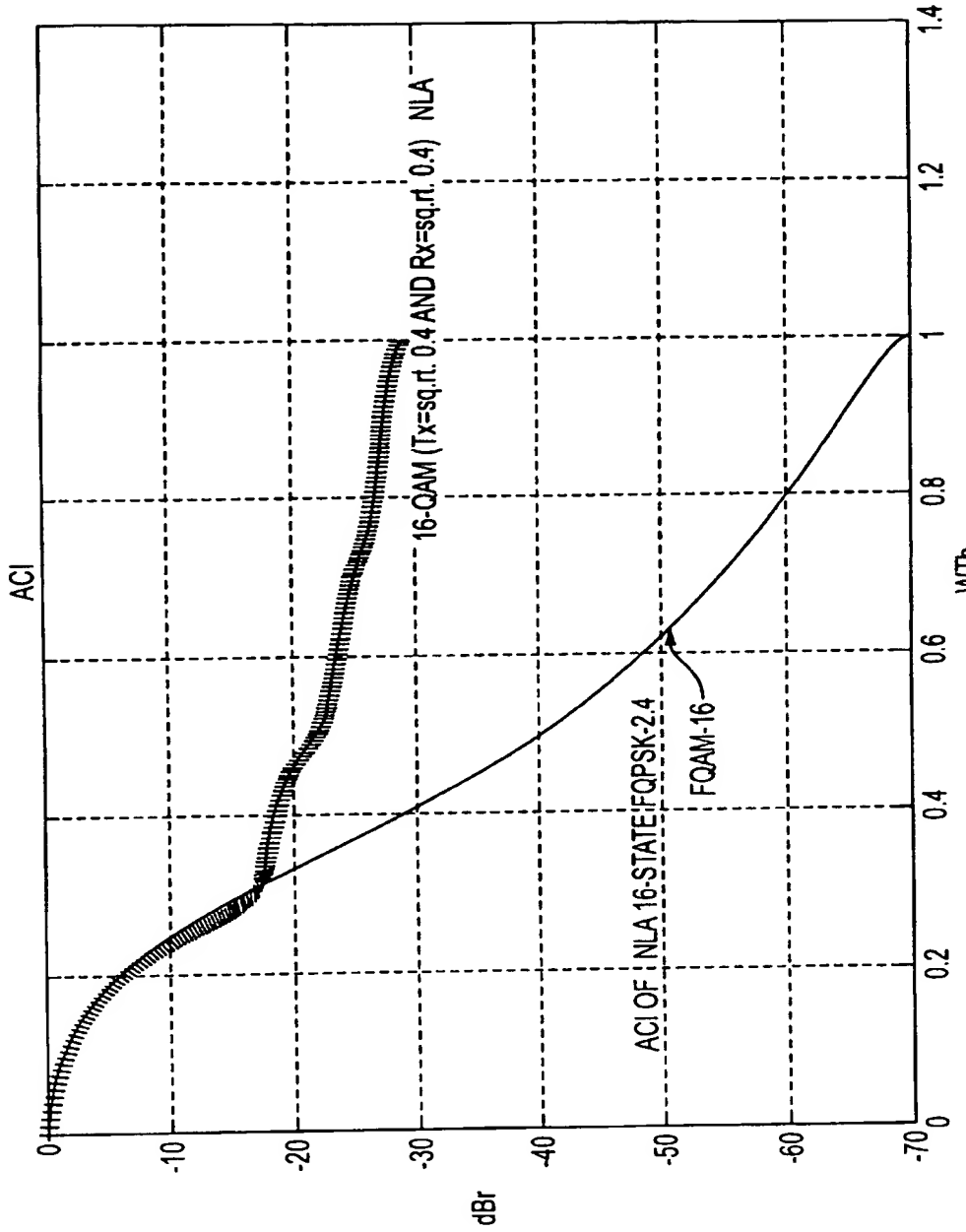

ACI
dBr
WTb
0
-10
-20
-30
-40
-50
-60
-70
0
0.2
0.4
0.6
0.8
1
1.2
1.4
16-QAM (Tx=sq.rt. 0.4 AND Rx=sq.rt. 0.4) NLA
ACI OF NLA 16-STATE FQPSK-2.4
FQAM-16

FIG. 28

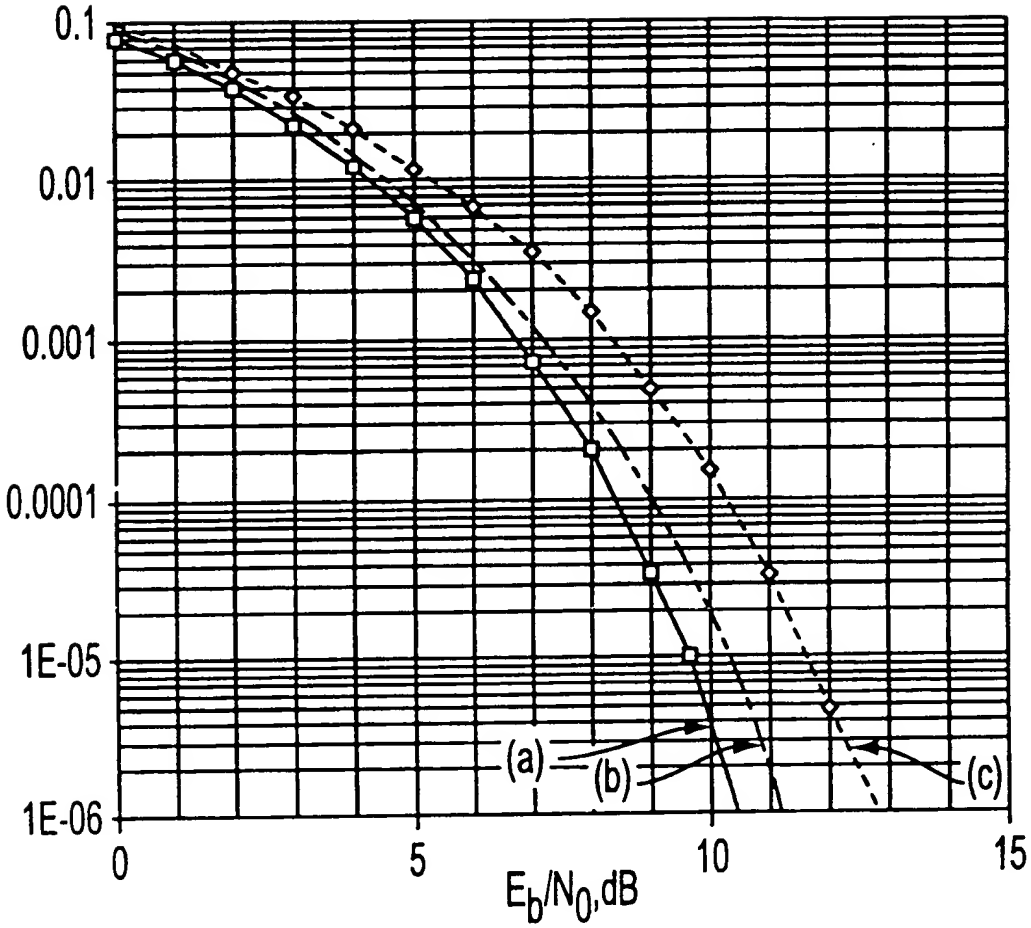


FIG. 29

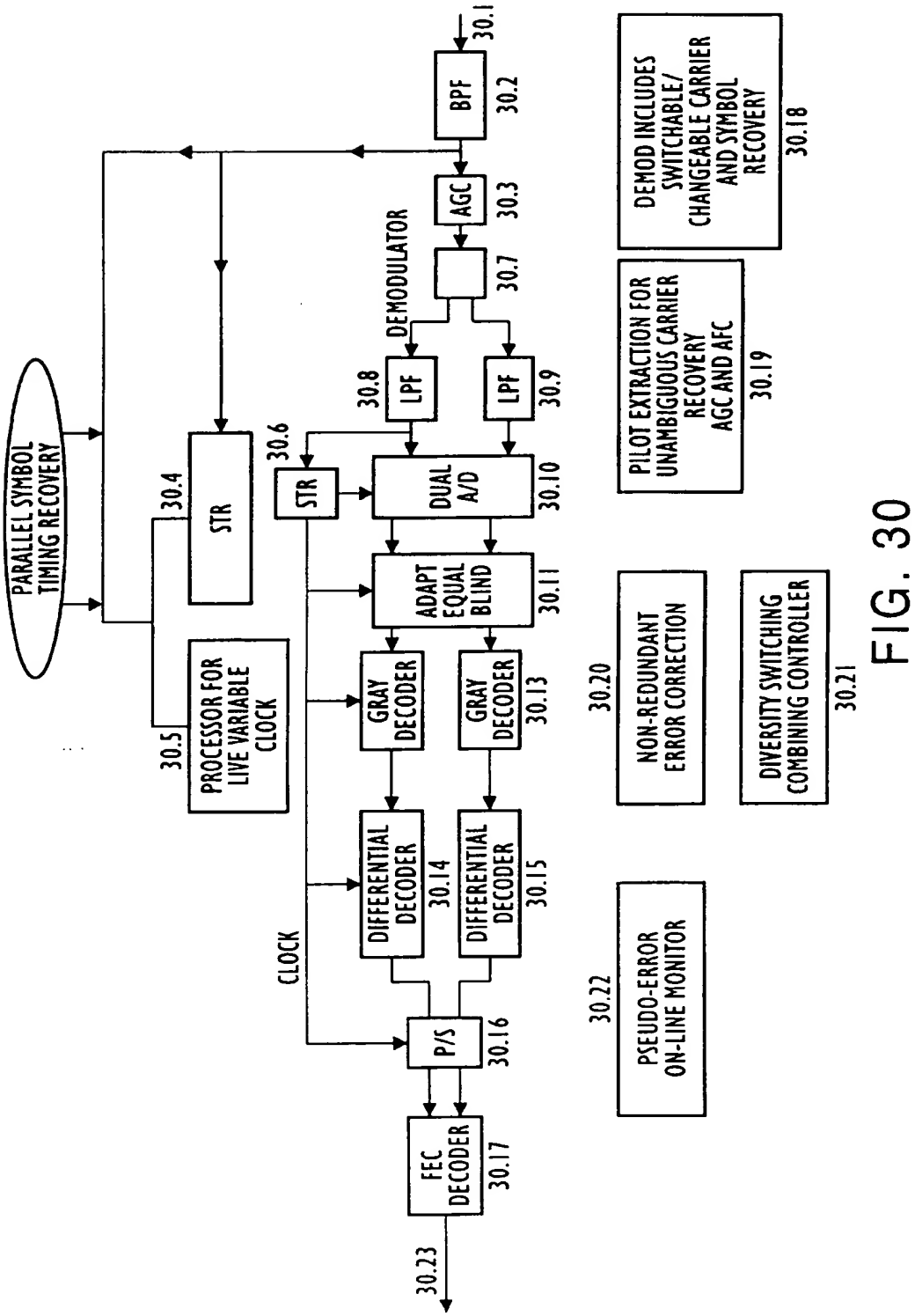

PARALLEL SYMBOL TIMING RECOVERY
30.1
BPF
30.2
AGC
30.3
DEMODULATOR
30.7
30.8
LPF
LPF
30.9
30.4
STR
30.6
STR
DUAL A/D
30.10
ADAPT EQUAL BLIND
30.11
30.5
PROCESSOR FOR LIVE VARIABLE CLOCK
GRAY DECODER
GRAY DECODER
30.13
CLOCK
DIFFERENTIAL DECODER
30.14
DIFFERENTIAL DECODER
30.15
P/S
30.16
FEC DECODER
30.17
30.23
DEMOD INCLUDES SWITCHABLE/ CHANGEABLE CARRIER AND SYMBOL RECOVERY
30.18
PILOT EXTRACTION FOR UNAMBIGUOUS CARRIER RECOVERY AGC AND AFC
30.19
30.20
NON-REDUNDANT ERROR CORRECTION
DIVERSITY SWITCHING COMBINING CONTROLLER
30.21
30.22
PSEUDO-ERROR ON-LINE MONITOR

FIG. 30

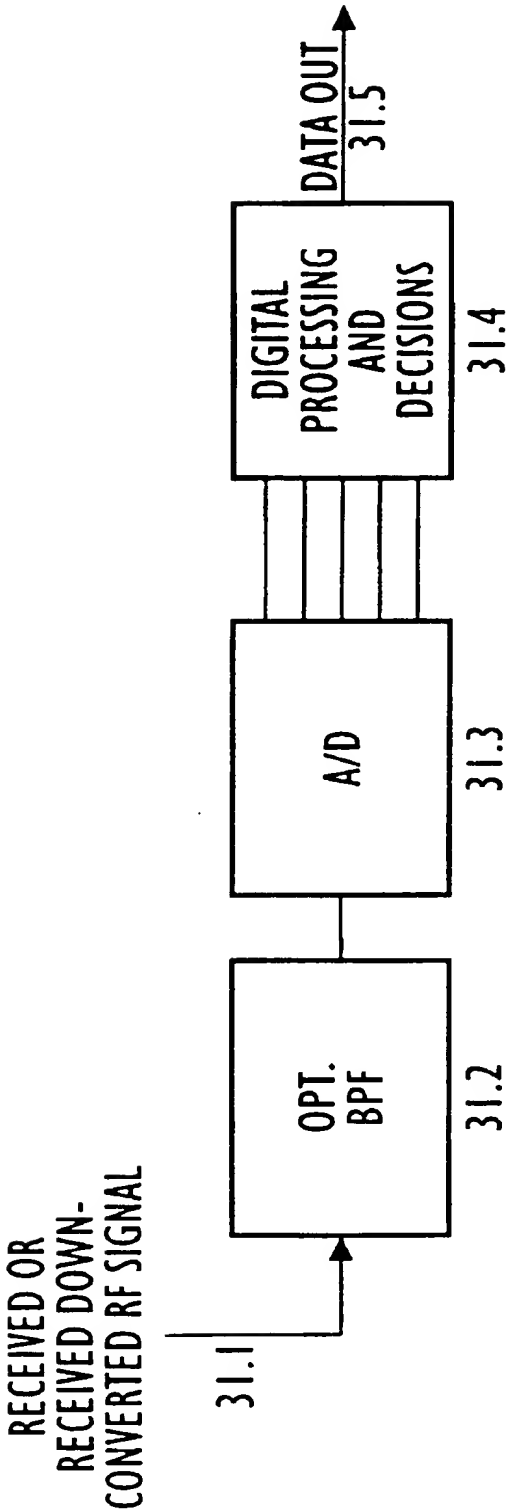

RECEIVED OR
RECEIVED DOWN-
CONVERTED RF SIGNAL
31.1
OPT.
BPF
31.2
A/D
31.3
DIGITAL
PROCESSING
AND
DECISIONS
31.4
DATA OUT
31.5

FIG. 31

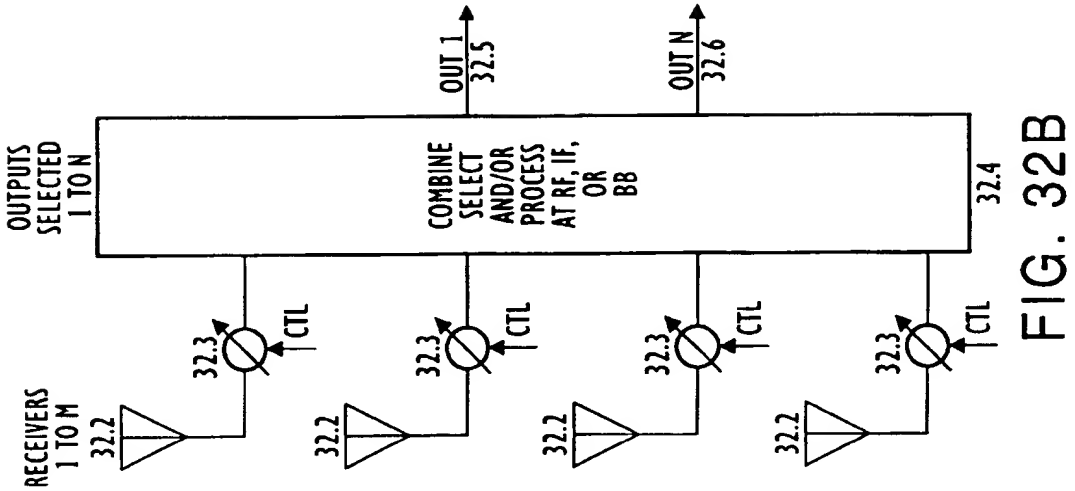


FIG. 32B

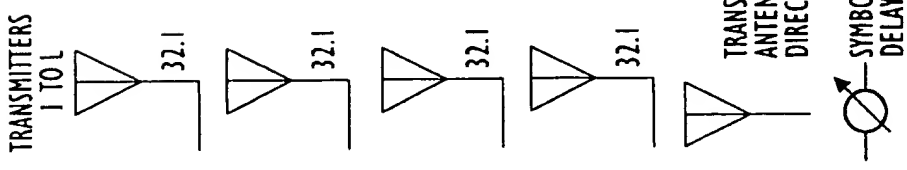


FIG. 32A

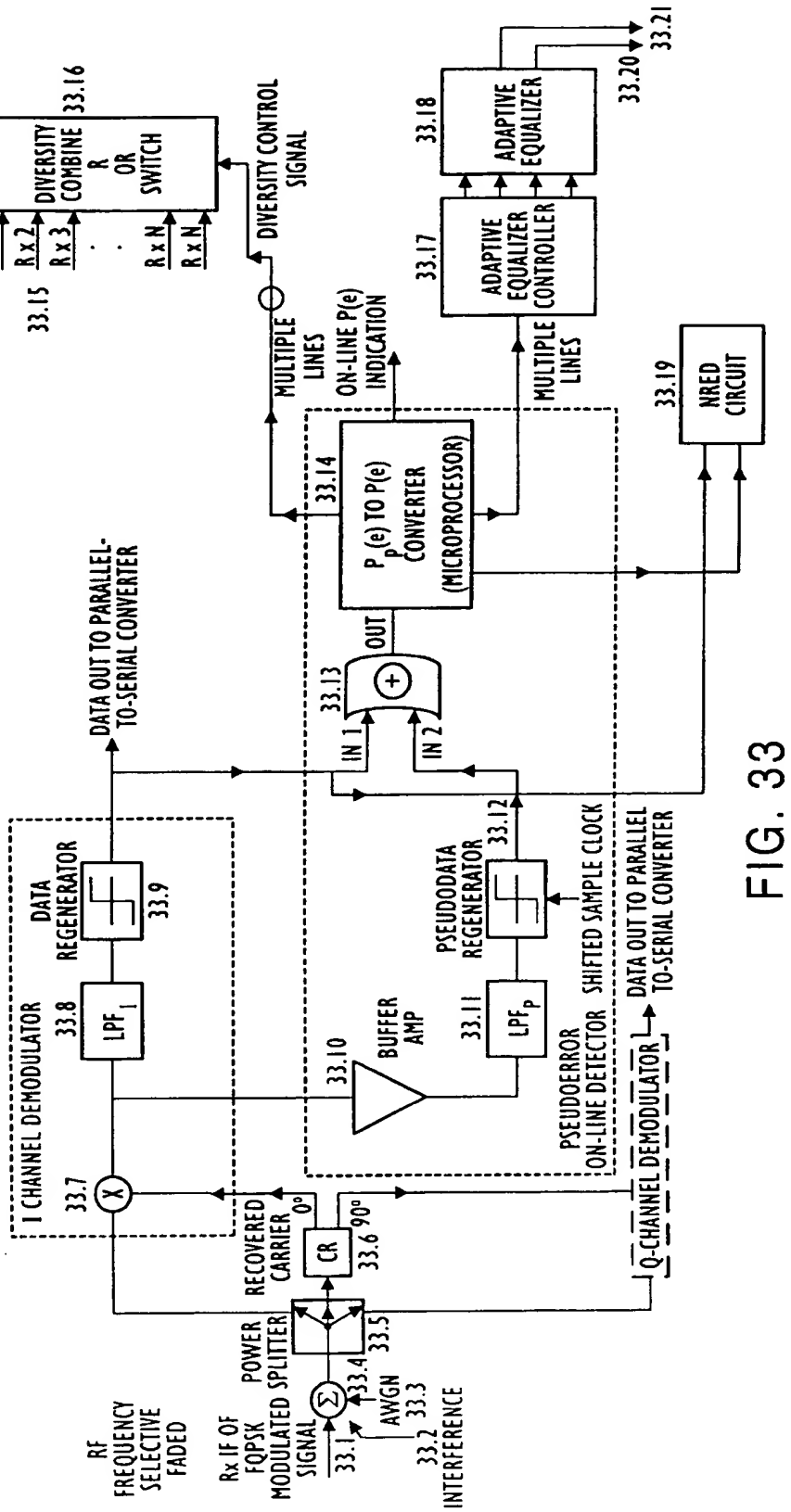

RF FREQUENCY SELECTIVE FADED
Rx IF OF FQPSK MODULATED SIGNAL
33.1
AWGN
33.3
33.2 INTERFERENCE
33.4
POWER SPLITTER
33.5
RECOVERED CARRIER
0°
90°
CR
33.6
33.7
I CHANNEL DEMODULATOR
33.8
LPF I
DATA REGENERATOR
33.9
DATA OUT TO PARALLEL-TO-SERIAL CONVERTER
33.10
BUFFER AMP
33.11
LPF P
PSEUDODATA REGENERATOR
33.12
SHIFTED SAMPLE CLOCK
PSEUDOERROR ON-LINE DETECTOR
Q-CHANNEL DEMODULATOR
DATA OUT TO PARALLEL TO-SERIAL CONVERTER
33.13
IN 1
IN 2
OUT
33.14
P(e) TO P(e) CONVERTER (MICROPROCESSOR)
MULTIPLE LINES
ON-LINE P(e) INDICATION
MULTIPLE LINES
33.15
Rx 1
Rx 2
Rx 3
Rx N
Rx N
33.16
DIVERSITY COMBINE OR SWITCH
DIVERSITY CONTROL SIGNAL
33.17
ADAPTIVE EQUALIZER CONTROLLER
33.18
ADAPTIVE EQUALIZER
33.19
NRED CIRCUIT
33.20
33.21

FIG. 33

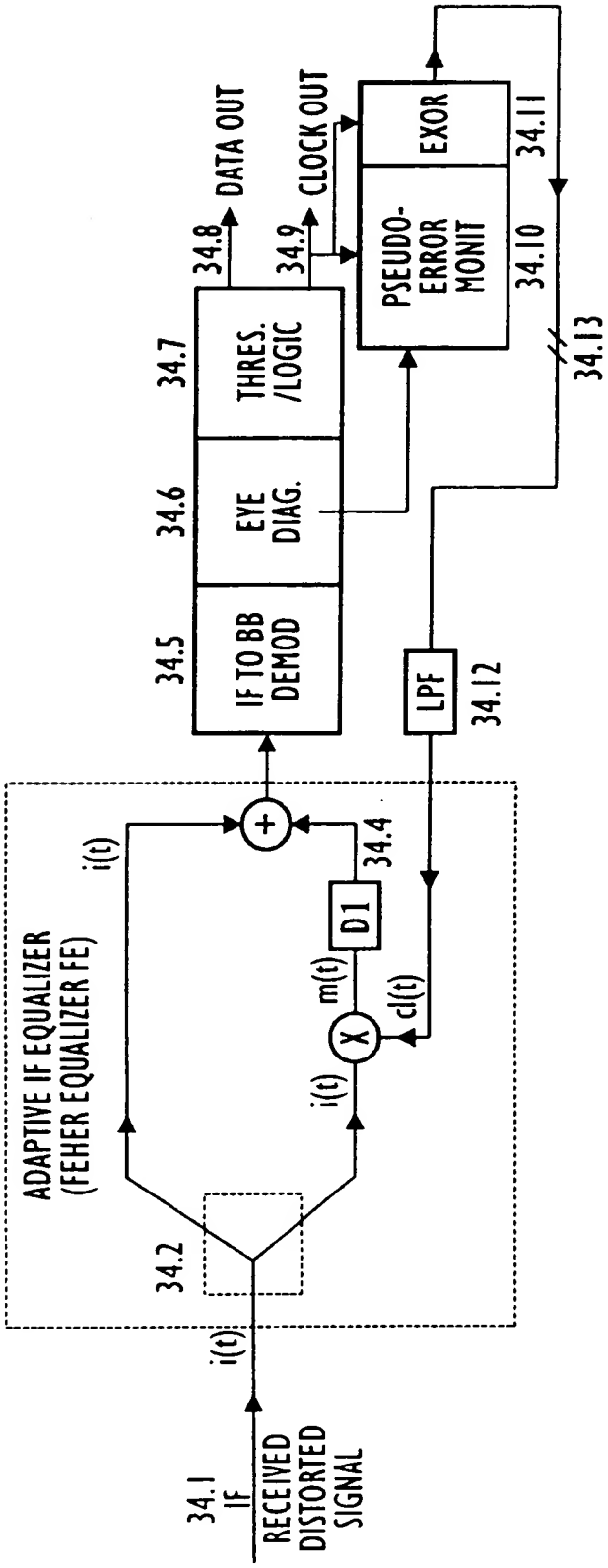

34.1
IF
RECEIVED
DISTORTED
SIGNAL
i(t)
ADAPTIVE IF EQUALIZER
(FEHER EQUALIZER FE)
34.2
i(t)
34.4
D1
m(t)
cl(t)
i(t)
LPF
34.12
34.5
IF TO BB
DEMOD
34.6
EYE
DIAG.
34.7
THRES.
/LOGIC
34.8
DATA OUT
34.9
CLOCK OUT
34.10
PSEUDO-
ERROR
MONIT
34.11
EXOR
34.13

FIG. 34

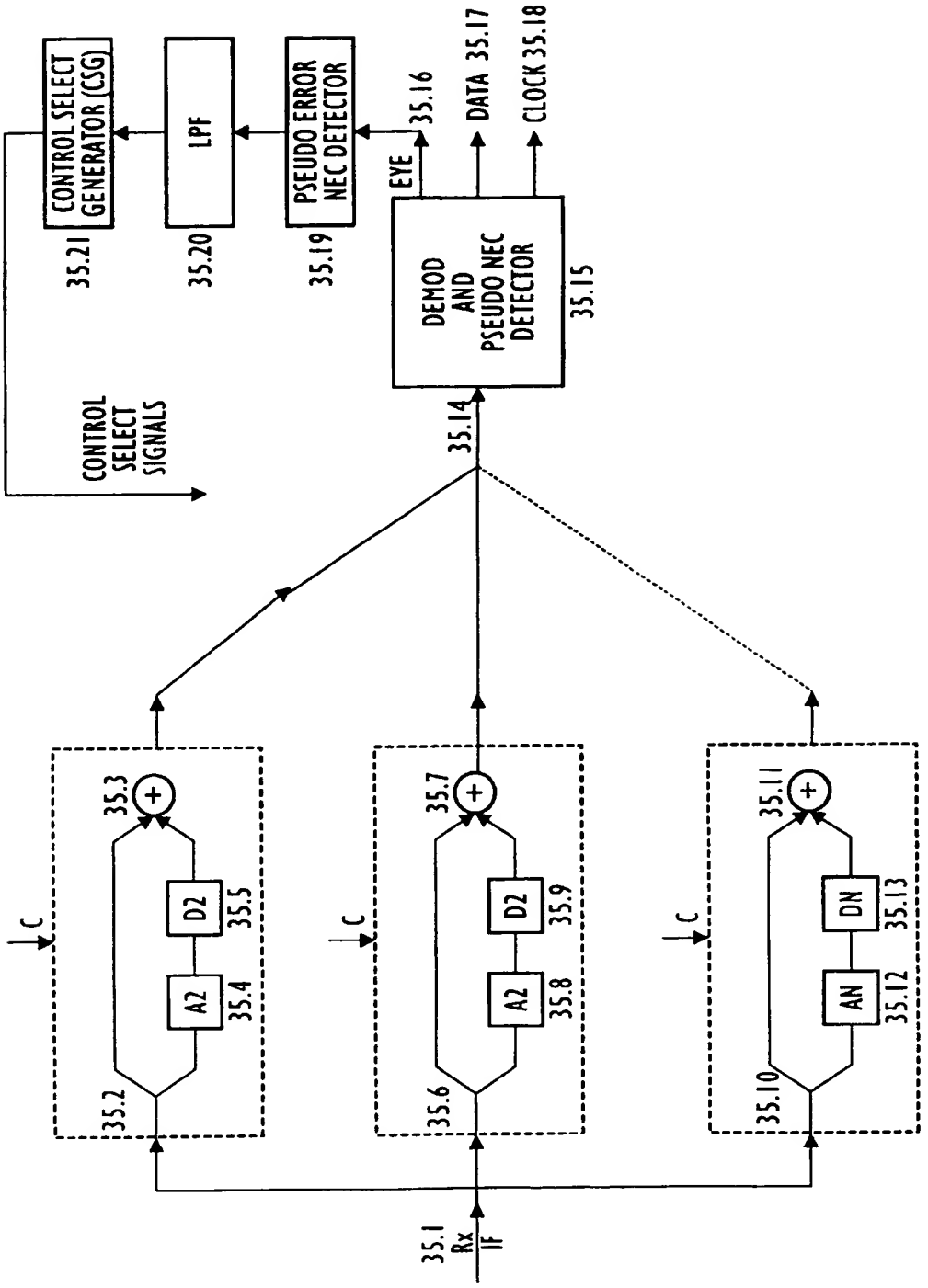

CONTROL SELECT GENERATOR (CSG)
LPF
PSEUDO ERROR NEC DETECTOR
EYE
35.16
DATA 35.17
CLOCK 35.18
DEMOD AND PSEUDO NEC DETECTOR
35.15
35.21
35.20
35.19
CONTROL SELECT SIGNALS
35.14
C
35.3
D2
35.5
A2
35.4
35.2
35.7
35.9
35.8
35.6
35.11
DN
35.13
AN
35.12
35.10
35.1
Rx
IF

FIG. 35

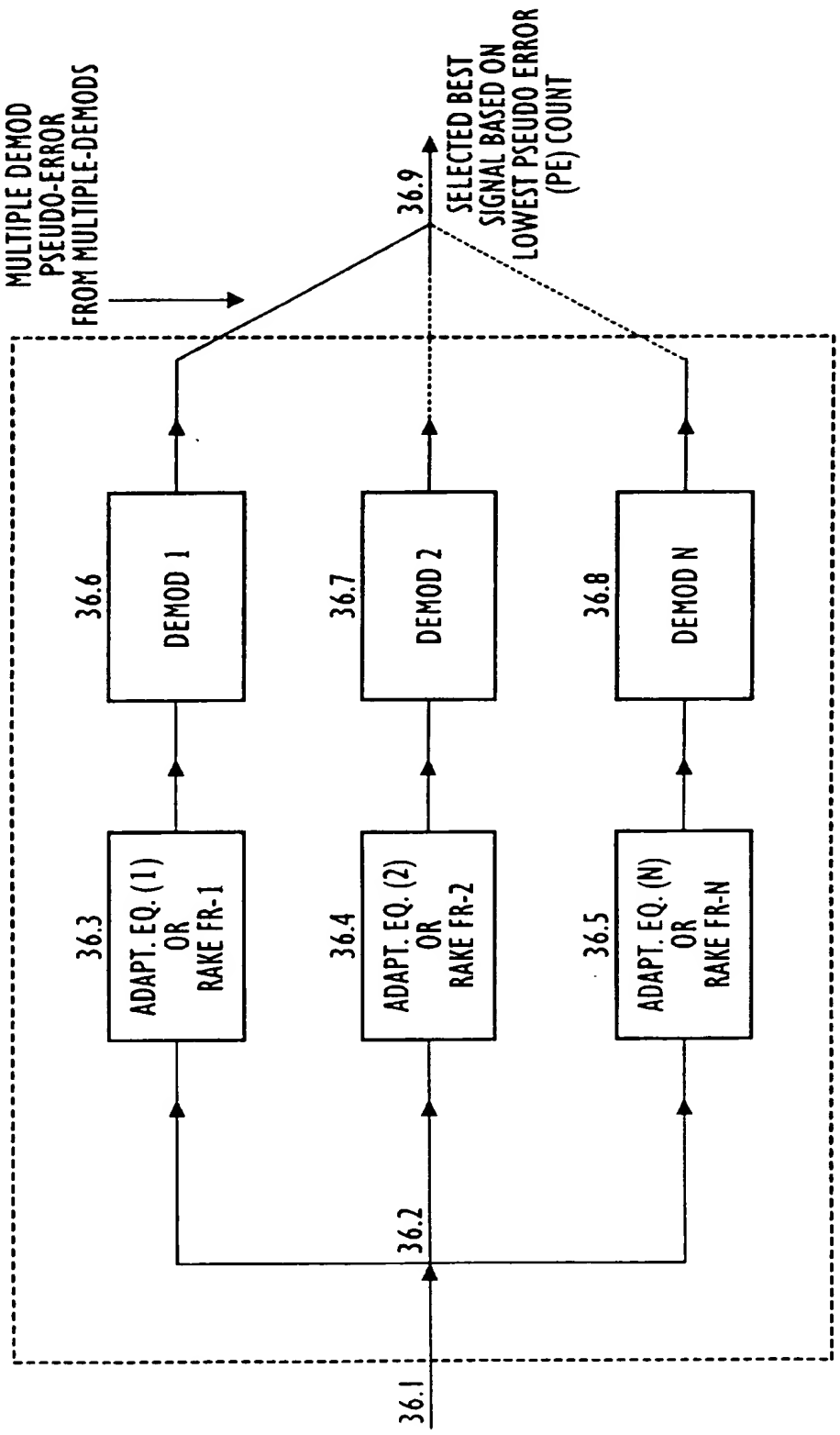

MULTIPLE DEMOD PSEUDO-ERROR FROM MULTIPLE-DEMODS
36.9
SELECTED BEST SIGNAL BASED ON LOWEST PSEUDO ERROR (PE) COUNT
36.6
DEMOD 1
36.7
DEMOD 2
36.8
DEMOD N
36.3
ADAPT. EQ. (1) OR RAKE FR-1
36.4
ADAPT. EQ. (2) OR RAKE FR-2
36.5
ADAPT. EQ. (N) OR RAKE FR-N
36.2
36.1

FIG. 36

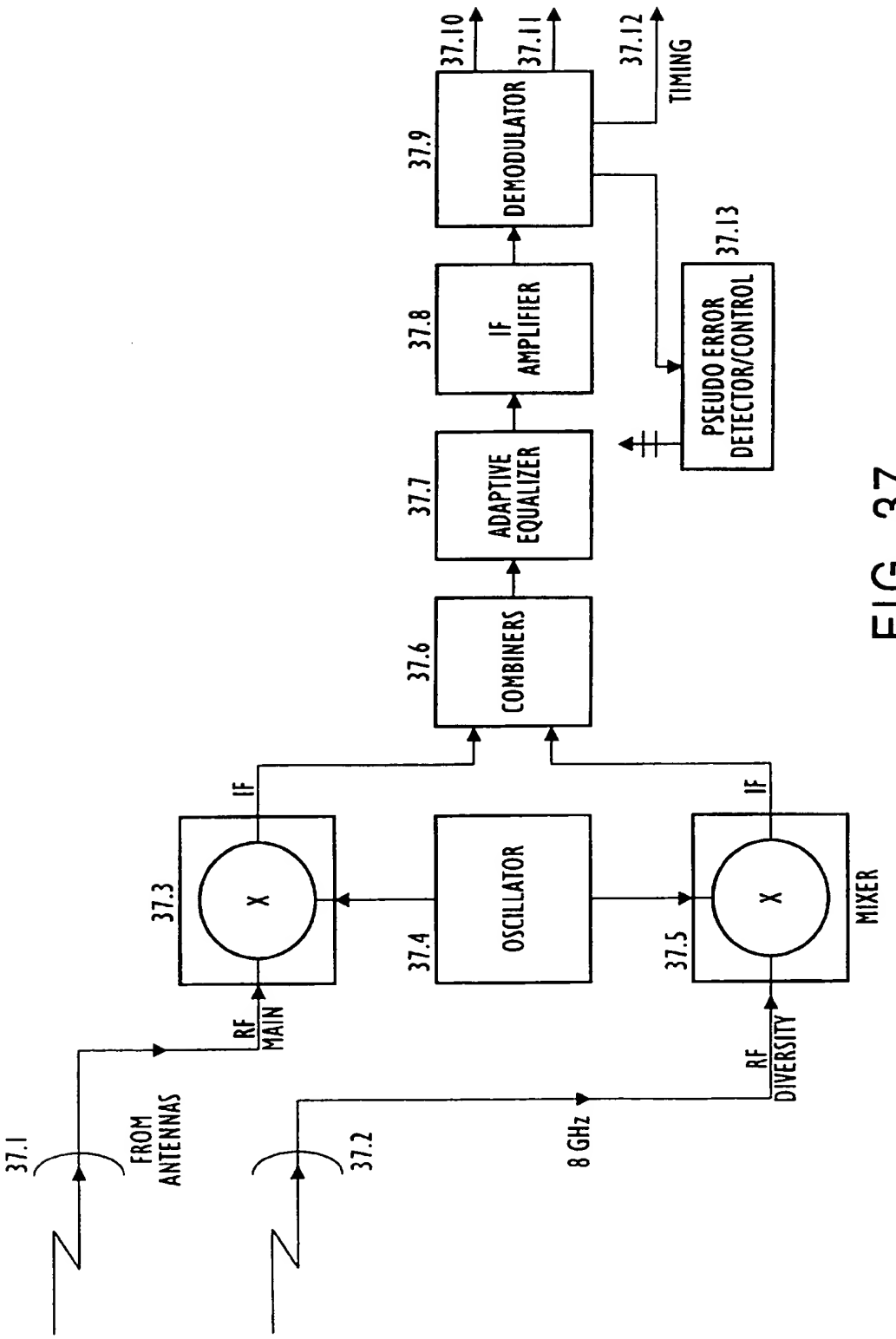

37.1
FROM ANTENNAS
37.2
8 GHz
RF MAIN
RF DIVERSITY
37.3
X
37.4
OSCILLATOR
37.5
X
MIXER
IF
IF
37.6
COMBINERS
37.7
ADAPTIVE EQUALIZER
37.8
IF AMPLIFIER
37.9
DEMODULATOR
37.10
37.11
37.12
TIMING
37.13
PSEUDO ERROR DETECTOR/CONTROL

FIG. 37

BIT RATE AGILE THIRD-GENERATION WIRELESS CDMA, GSM, TDMA AND OFDM SYSTEM

RELATED APPLICATIONS

This application claim the benefit under 35 U.S.C. 119(e) of U.S. Provisional Patent Application Serial No. 60/095,943 entitled "FQPSK TRANSCEIVERS" filed 10 Aug. 1998 [PP3]; and incorporated herein by reference.

Other related U.S. Patent Applications are co-pending U.S. Utility patent application Ser. No. 09/111,723 [PP1] filed 8 Jul. 1998 and entitled "FMOD TRANSCEIVERS INCLUDING CONTINUOUS AND BURST OPERATED TDMA, FDMA, SPREAD SPECTRUM CDMA, WCDMA AND CSMA"; United States Provisional Patent Application Serial No. 60/098,612 [PP2] entitled "FK MODULATION AND TRANSCEIVERS INCLUDING CLOCK SHAPING PROCESSORS" filed 31 Aug. 1998; each of which is hereby incorporated by reference.

FIELD OF THE INVENTION

This invention relates generally to Bit Rate Agile (BRA) signal processors; more particularly to cross-correlated signal processors for increasing RF spectral and power efficiency of modulated transmitted signals including but not limited to digital binary, digital multilevel, and/or analog modulated signals operated in linearized and in power-efficient Non-Linearly Amplified (NLA) systems; and most particularly to BRA and RF Agile Cascaded Time Constrained Signal (TCS) response and Long Response (LR) filtered and Mis-Matched (MM) filtered (ACM) quadrature phase, frequency and amplitude modulated Transmitter, Receiver, and Transceiver systems having these characteristics and methods and procedures provided thereby.

BACKGROUND OF THE INVENTION

The most important objectives of wireless communications, broadcasting, telemetry, infrared and in general "radio" systems as well as "wired" systems include: power and bandwidth or spectrum efficiency combined with robust Bit Error Rate (BER) performance in a noisy and/or strong interference environment. These system objectives are specified in numerous systems including wireless communications and cellular systems, satellite systems, mobile and telemetry systems, broadcasting systems, cable, fiber optics and practically all communication transmission systems. A partial list of publications, references, and patents are provided separately below. The cited publications, references [1–23] and patents [P1–P8], and the references within the aforementioned publications contain definitions and descriptions of many terms used in this new patent disclosure and for this reason these conventional terms and definitions will be described only briefly, and highlighted on a case by case basis.

Robust or high performance Bit Error Rate (BER) specifications and/or objectives are frequently expressed in terms of the required BER as a function of Energy per Bit (Eb) divided by Noise Density or simply noise (No), that is, by the BER=f(Eb/No) expression. Low cost, reduced size, and compatibility and/or interoperability with other conventional or previously standardized systems, also known as "legacy systems," are highly desired. Several standardization organizations have adopted modulation techniques such as conventional Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), Offset Quadrature Phase Shift Keying (OQPSK) also designated as Staggered Quadrature Phase Shift Keying (SQPSK), and pi/4-QPSK (or π/4-QPSK) techniques including differential encoding variations of the same. See publications [1–23] and referenced patents [P1–P8] for examples and further description. For spectrally or spectrum efficient signaling (such as band-limited signaling), these conventional methods exhibit a large envelope fluctuation of the modulated signal, and thus have a large increase in peak radiated power relative to the average radiated power. For these reasons such systems are not suitable for BRA, robust BER performance NLA operated RF power efficient systems.

Within the present state of the technology, for numerous BRA Transceiver applications, it is not practical to introduce band-pass filtering after the NLA power efficient Radio Frequency (RF) final amplifier stage. Here we are using the term "Radio Frequency" (RF) in its broadest sense, implying that we are dealing with a modulated signal. The RF could be, for example, as high as the frequency of infrared or fiber optic transmitters; it could be in the GHz range, for example, between 1 Ghz and 300 GHz or more, or it could be in the MHz range, for example, between about 1 Mhz and 999 MHz, or just in the kHz range. The term RF could even apply to Quadrature Modulated (abbreviated "QM" or "QMOD") Base-Band (BB) signals or to Intermediate Frequency (IF) signals.

In conventional BPSK, QPSK, OQPSK or SQPSK, and differentially-encoded phase-shift keying systems variants of these systems, such as DBPSK and DQPSK, as well as in pi/4-DQPSK and trellis coded QPSK and DQPSK, large envelope fluctuations require linearized (LIN) or highly linear transmitters including frequency up-converters and RF power amplifiers and may require expensive linear receivers having linear Automatic Gain Control (AGC) circuits. A transmitter NLA reduces the time domain envelope fluctuation of conventional QPSK type of band-limited signals and this reduction of the envelope fluctuation, being a signal distortion, is the cause of spectral restoration or spectral regrowth and the cause of unacceptably high levels of out-of-band spectral energy transmission, also known as out-of-band interference. Additionally, for conventional BPSK, QPSK, and also Quadrature Amplitude Modulation number (QAM) signals, undesired in-phase channel (I) to quadrature channel (Q) crosstalk is generated. This crosstalk degrades the BER=f(E_b/N_o) performance of the modulated radio transmitter.

Experimental work, computer simulation, and theory documented in many recent publications indicates that for band-limited and standardized BPSK, QPSK, OQPSK or SQPSK or pi/4-QPSK, and QAM system specifications, very linear amplifiers are required to avoid the pitfalls of spectral restoration and of BER degradation. Linearized or linear amplifiers are less RF power efficient (during the power "on" state, power efficiency being defined as the transmit RF power divided by DC power), are considerably more expensive and/or having less transmit RF power capability, are larger in size, and are not as readily available as NLA amplifiers. The advantages of NLA over LIN amplifiers are even more dramatic at higher RF frequencies, such as frequencies above about 1 GHz for applications requiring low dc voltage, for example applications or systems operating on size "AA" batteries having only 1.5 Volt dc and for high RF modulated power requirements, for example transmit RF power in the 0.5 Watt to 100 Watt range.

Published references [P1 to P8] and [1 to 23] include additional background information. These references

include descriptions of binary-state and multiple-state Transmitter/Receiver (Transceiver) or for short ("TR") systems that are suitable for NLA. In the aforementioned references Processors, Modems, Transmitters, Receivers and Transceivers, suitable for NLA, have been described, defined and designated as first generation of Feher patented Quadrature Shift Keying (FQPSK). For example, in reference [22] published on May 15, 1999 the authors Drs. M. K. Simon and T. Y. Yan of JPL/NASA-Caltech present a detailed study of Unfiltered Feher-Patented Quadrature Phase Shift Keying (FQPSK). In references [1–22] and patents #[P1–P8] numerous first generation FQPSK technology based terms, and terms other than the FQPSK abbreviation/acronym have been used. In addition to FQPSK Transceivers, these first generation of systems have been also described and/or defined as: Feher's Minimum Shift Keying (FMSK), Feher's Frequency Shift Keying (FFSK), Feher's Gaussian Minimum Shift Keying (FGMSK), Feher's Quadrature Amplitude Modulation (FQAM) and/or Feher's (F) Modulation/Amplification (FMOD). Additionally terms such as Superposed Quadrature Amplitude Modulation (SQAM), Intersymbol Interference and Jitter Free (IJF) and/or IJF-OQPSK have been also described in Feher et al.'s prior patents and publications, each of which is incorporated by reference.

In the cited patents and other references, among the aforementioned abbreviations, acronyms, designation, terms and descriptions the "FQPSK" abbreviation/term has been most frequently used to describe in most generic terms one or more of these afore described Feher or Feher et al. first generation of Non-Linearly Amplified (NLA) inventions and technologies. The 1st generation of FQPSK systems have significantly increased spectral efficiency and enhanced end-to-end performance as compared to other NLA systems. RF power advantages, robust BER performance, and NLA narrow spectrum without the pitfalls of conventional BPSK and DBPSK, QPSK and OQPSK have been attained with these 1st generation FQPSK systems and methods. The generic 1st generation terms such as FQPSK, as well as other previously mentioned terms/acronyms are retained and used in this description to describe the new BRA, Code Selectable (CS), Modem Format Selectable (MFS) and modulation-demodulation Mis-Matched (MM) filtered architectures and embodiments of "2nd generation" FQPSK Transceivers.

While these earlier issued patents and publications describe material of a background nature, they do not disclose the original new enhanced performance bit rate agile and modulation agile/selectable technologies disclosed in this new invention.

PARTIAL LIST OF RELEVANT LITERATURE

Several references, including United States Patents, International or Foreign Patents, publications, conferences proceedings, and other references are identified herein to assist the reader in unerstanding the context in which the invention is made, some of the distinctions of the inventive structures and methods over that which was known prior to the invention, and advantages over the invention. No representation is made as to whether the contents of the cited references represent prior-art as several of the cited references have a date after the effective filing date (priority date) of this patent application. This list is intended to be illustrative rather than exhaustive.

United States Patents

[P1] U.S. Pat. No. 5,784,402 Issued July 1998 to Feher
[P2] U.S. Pat. No. 5,491,457 Issued February 1996 to Feher
[P3] U.S. Pat. No. 4,720,839 Issued January 1988 to Feher et al.
[P4] U.S. Pat. No. 4,644,565 Issued February 1987 to Seo/Feher
[P5] U.S. Pat. No. 4,567,602 Issued January 1986 to Kato/Feher
[P6] U.S. Pat. No. 4,350,379 Issued September 1982 to Feher
[P7] U.S. Pat. No. 4,339,724 Issued July 1982 to Feher
[P8] U.S. Pat. No. 3,954,926 Issued March 1976 to Feher

Foreign Patent Documents

[PF1] Canadian Patent No. 1130871 August 1982
[PF2] Canadian Patent No. 1211517 September 1986
[PF3] Canadian Patent No. 1265851 February 1990

Other Publications

1. Feher, K.: *Wireless Digital Communications: Modulation Spread Spectrum*. Prentice Hall, 1995.
2. Feher, K.: *Digital Communications: Satellite/Earth Station Engineering*. Prentice Hall, 1983. Available from Crestone Engineering—Noble Publishing, 2245 Dillard Street, Tucker, Ga. 30084.
3. Feher, K.: *Advanced Digital Communications: Systems and Signal Processing*. Prentice Hall, 1987. Available from Crestone Engineering—Noble Publishing, 2245 Dillard Street, Tucker, Ga. 30084.
4. Feher, K.: *Digital Communications: Microwave Applications*. Prentice Hall 1981. Since 1997 available from Crestone Engineering—Noble Publishing, 2245 Dillard Street, Tucker, Ga. 30084.
5. Feher, K. and Engineers of Hewlett-Packard: *Telecommunications Measurements, Analysis, and Instrumentation*: Prentice Hall 1987. Since 1997 reprints have been available from Crestone Engineering—Noble Publishing, 2245 Dillard Street, Tucker, Ga. 30084.
6. Feher, K., Emmenegger, H.: "FQPSK Use for Electronic News Gathering (ENG), Telemetry and Broadcasting," *Proc. of the National Association of Broadcasters* NAB'99 Broadcast Engineering Conference, Las Vegas, Apr. 19–22, 1999.
7. Feher, K.: "FQPSK Doubles Spectral Efficiency of Operational Systems: Advances, Applications, Laboratory and Initial Air-to-Ground Flight Tests" (Date of Submission: Aug. 14, 1998). *Proc. of the International Telemetry Conference*, ITC-98 ITC/USA 98, San Diego, Calif., Oct. 26–29, 1998.
8. W. Gao, S. H. Wang, K. Feher: "Blind Equalization for FQPSK and FQAM Systems in Multipath Frequency Selective Fading Channels," *Proc. Internat. Telemetry Conf.* ITC/USA'99 Oct. 25–28, 1999, Las Vegas, Nev.
9. Terziev, G., Feher, K.: "Adaptive Fast Blind Feher Equalizers (FE) for FQPSK," *Proc. Of the International Telemetry Conference* ITC/USA'99, Oct. 25–28, 1999, Las Vegas, Nev.
10. Feher, K.: "FQPSK Transceivers Double the Spectral Efficiency of Wireless and Telemetry Systems" *Applied Microwave & Wireless Journal*, Jun. 1998.
11. Seo, J-S. and K. Feher: "Bandwidth Compressive 16-State SQAM Modems through Saturated Amplifiers," *IEEE Radio Commun., ICC'86*, Toronto, June 1986.

12. Kato, S. and K. Feher: "XPSK: A new cross-correlated PSK," *IEEE Trans. Com.*, May 1983.
13. Law, E. L., U.S. Navy: "Robust Bandwidth Efficient Modulation" *European Telemetry Conference, ETC-98*, Germany, May 1998.
14. Feher, K.: "FQPSK Doubles the Spectral Efficiency of Operational Telemetry Systems," *European Telemetry Conference, ETC-98*, May 1998, Germany.
15. Do, G. and K. Feher: "FQPSK-GMSK: Wireless System Tests an ACI Environment, " *Proc. of Wireless Symposium*, Santa clara, Calif., Feb. 9–13, 1998.
16. Law, E. and K. Feher: "FQPSK versus PCM/FM for Aeronautical Telemetry Applications: Spectral Occupancy and Bit Error Probability Comparisons" *Proc. of ITC-97*, Las Vegas, October 1997.
17. Feher, K "FQPSK Doubles Spectral Efficiency of Telemetry: Advances and Initial Air to Ground Flight Tests," ITC/USA 98, *Proc. of the Internat. Telemetry Conference*, San Diego, October 1998.
18. Law, E. and K. Feher: "FQPSK versus PCM/FM for Aeronautical Telemetry Applications; Spectral Occupancy and Bit Error Probability Comparisons," *Proc. of the Internat. Telemetry Conf.*, Las Vegas, Nev., Oct. 27–30, 1997.
19. Martin, W. L., T-Y. Yan, L. V. Lam: "Efficient Modulation Study at NASA/JPL," *Proc. of the Tracking, Telemetry & Command Systems Conference*, European Space Agency (ESA), June 1998.
20. Law, E. L., ITC-98 Session Chair: "RCC Alternate Standards and IRIG106 update," Briefings by DoD during ITC/USA 98 *Internat. Telemetry Conference*, San Diego, October 1998.
21. K. Feher: "FQPSK Doubles Spectral Efficiency of Operational Systems: Advances, Applications, Laboratory and Initial Air to Ground Flight Tests", File: ITC.98. Final Paper. Rev. 5. Aug. 14, 1998 (Date of Submission) for publication in *the Proc. of the International Telemetering Conference*, ITC-98; San Diego, Oct. 26–29, 1998
22. Simon, M. K, Yan, T. Y. "Performance Evaluation and Interpretation of Unfiltered Feher-Patented Quadrature Phase-Shift Keying (FQPSK)," California Institute of Technology, JPL-NASA publication, *TMD Progress Report* 42–137, Pasadena, Calif., May 15, 1999.
23. Winters, J. H.: "Adaptive Antenna Arrays for Wireless Systems," *Tutorial Notes presented/distributed at the* 1999 *IEEE Vehicular Technology Conference*, Houston, Tex., May 16, 1999.

SUMMARY OF THE INVENTION

This invention includes disclosure of new and/original spectral efficient and RF power efficient-high performance technologies, new architectures, embodiments and new Bit Rate Agile (BRA) implementation of 2^{nd} generation FQPSK Transceivers. These inventive structures, methods, and technologies are suitable for a large class of implementations and applications. Numerous embodiments of the inventive structures and methods are enabled. These include cost effective solutions for BRA, Modulation and Demodulation (Modem) Format Selectable (MFS) and Coding Selectable (CS) processors, modulators/demodulators, Transceivers, having agile/tunable RF frequency embodiments and are suitable for power efficient NLA systems.

The terms abbreviations and descriptions used in the 1^{st} generation of Feher et. al inventions, highlighted in the "Background of the Invention" section, as well as other previously identified terms/acronyms and abbreviation and in particular FQPSK and related terms, used in the cited references, are retained and/or slightly modified and are used relative to this disclosure of the new invention to describe second generation "2^{nd} generation" BRA architectures and embodiments of FQPSK, FGMSK and FQAM Transceivers. This disclosure contains embodiments for further significant spectral savings and performance enhancements, and new functions and architectures, which were not, included in the referenced prior art patents, inventions and publications.

BRA or "Bit Rate Agile" abbreviation and term describes technologies, implementations, embodiments suitable for design, use and applications in which the information rate, source rate, or the often used alternative terms "bit rate", "symbol rate", or "data rate" may be selectable or programmable by the user or by one or more control signal(s). Bit Rate Agile (BRA) systems may be programmable by software or have predetermined or "selectable," i.e., "agile" bit rate applications. The term "bit rate agility" refers to variable and/or flexible selectable bit rates (again bit rate, symbol rate, data rate, information rate, source rate, or equivalent); the bit rates could be selected on a continuous fashion in small increments and/or in steps. These systems are designated as BRA (or Bit Rate Agile) systems. BRA, MFS, and CS systems requirements are increasing at a rapid rate.

Changeable (or variable, or selectable) amounts of cross-correlation between Time Constrained Signal (TCS) response processors and/or combined TCS and Long Response (LR) processor and/or post processor filters of in-phase (I) and quadrature (Q) phase signals of BRA Transceivers, MFS and CS baseband signal processing implementations and architectures for tunable RF frequency embodiments having enhanced spectral efficiency and end-to-end performance are disclosed. These new BRA, MFS and CS classes of FQPSK signal processors, modems and transceivers, with Adaptive Antenna Arrays (AAA) and RF power efficient amplifiers and entire Transceivers, operated in fully saturated or NLA mode, with intentionally Mis-Matched (MM) modulation and demodulation filters, transmit BRA and receive BRA filters/processors, disclosed herein, attain high performance advantages and significant spectral savings.

A changeable amount of cross-correlation between the BRA and MFS Time Constrained Signal (TCS) response processor and/or combined TCS and Long Response (LR) processor and/or post processor filters of the transmitter with selectable MM between the BRA transmitter and BRA receiver and CS processors, including single and separate in-phase (I) and quadrature (Q) signal storage/readout generators and single and/or separate I and Q channel D/A architectures and a bank of switchable filters for cross-correlated BRA, MFS and CS formats are also disclosed.

These new classes of 2^{nd} generation of FQPSK signal processors, modems and transceivers, with Adaptive Antenna Arrays (AAA) and RF power efficient amplifiers and entire Transceivers, operated in BRA, MFS and CS fully saturated NLA mode, or with LIN mode with intentionally Miss-Matched (MM) transmit BRA and receive BRA filters/processors, disclosed herein, have robust performance and significant spectral saving advantages.

In addition to digital embodiments, BRA analog cross-correlation implementations and combined digital-analog active and passive processors, for 2^{nd} generation FQPSK Transceivers are also disclosed. Subsets, within the generic 2^{nd} generation of the FQPSK family of processors, modems and transceivers are also designated as 2^{nd} generation BRA Feher's Minimum Shift Keying (FMSK), Feher's Gaussian

Minimum Shift Keying (FGMSK), Feher's Frequency Shift Keying (FFSK) and Feher's Quadrature Amplitude Modulation (FQAM).

Switched BRA, selectable Cross-Correlation (CC or Xcor) transmit and receive bandwidth Mis-Matched (MM) low-pass, band-pass and adaptive filter means and controller circuits and algorithms for preamble contained and differentially encoded and/or Forward Error Correction (FEC) with Redundant and Pseudo-Error (PE) based Non Redundant Detection (NED) implementations for FQPSK are also described.

The term "Mis-Matched" (MM) designates an intentional and substantial mis-match (MM) between the bandwidth and/or frequency or phase response of modulator filters and demodulator filters and/or mis-match (MM) between one or more implemented FQPSK filter(s) and the theoretical optimal performance minimum bandwidth Nyquist filters.

The term "Agile Cascaded Mis-Matched" (ACM) designates the BRA and RF agile ("flexible" or "tunable" RF frequency) cascaded TCS response and LR processor/filter(s) which are mis-matched within their respective application and/or use within this invention.

For NLA and for LIN amplifiers, selectable FQPSK filtering strategies in the transmitter and separately in the receiver lead to further spectral efficiency enhancements. Fast synchronization systems and robust efficient adaptive equalizers/adaptive switched systems are also disclosed.

The inventive structure and method includes transmit elements, receive elements, and transmit and receive elements, and may be applied to a variety of communication applications, including, but not limited to, wireless communications and cellular systems, satellite systems, mobile and telemetry systems, broadcasting systems, cable system, fiber optic systems, and more generally to nearly all communication transmission and/or receiving systems.

In one embodiment of the invention, a bit rate agile communication system is provided and includes a splitter receiving an input signal and splitting the input signal into a plurality of baseband signal streams, and a baseband signal processing network receiving the plurality of baseband signal streams and generating cross-correlated cascaded processed and filtered bit rate agile (BRA) in-phase and quadrature-phase baseband signals. In another embodiment, a quadrature modulator receiving and quadrature modulating the cross-correlated filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated output signal is also provided. In another embodiment, the baseband signal processing network includes a cross-correlator and at least one bit rate agile cascaded mis-matched (ACM) modulator filter.

In yet another embodiment, the invention provides a bit rate agile communication system including a baseband signal processing network receiving parallel baseband signal streams and generating combined Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals. In a variation of this embodiment, the inventive structure also includes a quadrature modulator receiving and quadrature modulating the Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated bit rate agile output signal.

In still another aspect, the invention provides a method for generating bit rate agile signals in a communication system. The method includes the steps of processing a plurality of signal streams to generate cross-correlated signals having changeable amounts of filtering for bit rate agile in-phase and quadrature-phase baseband signals. The inventive method may also include the step of receiving an input signal and converting the input signal into the plurality of signal streams. It may also optionally include the further step of modulating the cross-correlated filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated bit rate agile output signal.

In yet another aspect, the invention provides a method for generating bit rate agile signals in a signal transmission system, where the method includes the steps of receiving a plurality of signal streams, processing the plurality of signal streams to generate cascaded Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals; and modulating the Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated bit rate agile output signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1*a* is a diagram depicting an Agile Cascaded Mis-Matched (ACM) enhanced spectral efficiency, high performance Transmitter/Receiver (Transceiver) block diagram for a generic class of modulated systems.

FIG. 1*b* illustrates a somewhat generic Transmitter (Tx) block-implementation diagram of the invention for bit rate agile, selectable modulation formats, for hardware, firmware and/or software implementations including optional single and multi-tone inserts at one or more locations.

FIG. 2 depicts a Bit Rate Agile (BRA) integrated Base-Band Processor (BBP) with BRA post filters and BRA quadrature modulators. Signal splitting and serial/parallel BRA converters and TCS response processors in cascade with LR filter processors, which are MM enhancements and alternatives to referenced patents [P1 and P2] are also included.

FIG. 3 shows TCS response and cascaded LR filter baseband processor and filter preceded by a cross-correlator, and multiplexers for I and Q signal generation.

FIG. 4 illustrates coded baseband processing of FQPSK, FQAM, FGMSK and FMSK signals including non-redundant trellis coding of the baseband processed filtered I and Q signals.

FIG. 5 Time Constrained Signal (TCS) patterns, based on referenced patents [P4; P5; P7] are illustrated.

FIG. 6 shows an Agile Cascaded Mis-Matched (ACM) implementation block diagram embodiment of this invention with cascaded, switched transmit (Tx) and receive (Rx) Low-Pass- Filters (LPF) for BRA applications in conjunction with Cross-Correlated and other non-cross-correlated cascaded Time Constrained Signal (TCS) response processors and Long Response (LR) filters having substantially Mis-Matched (MM) modulation and demodulation filters.

FIG. 7 is an alternate embodiment- block diagram of the current invention, including Cross-Correlator in cascade with a 2^{nd} processor and with Digital to Analog (D/A) converters followed by spectral and pulse shaping bit rate agile LR filters, implemented by Low-Pass-Filters (LPF) in the I and Q channels of this Quadrature modulator.

FIG. 8 shows the implementation of an alternate Quadrature Modulator (QM) Transceiver having one or more Intersymbol-Interference and Jitter Free (IJF), Superposed Quadrature Amplitude Modulation (SQAM) or TCS response cascaded with LR response filter embodiments in the I and Q transmit Baseband Processor (BBP).

FIG. 9 illustrates a Non Return to Zero (NRZ) signal pattern, a TCS response pattern, a signal pattern of a TCS filtered by a conventional Low-Pass-Filter (LPF) resulting in cascaded TCS response and Long Response (LR) pulse patterns with some overshoots. In the non-Xcor case as well as in the Cross-Correlated case a Peak Limiter (PL) or gradual Soft Limiter or Xcor Soft Limiter reduces the amplitude peaks. The LR filter extends the TCS response to multiple pulses and may introduce additional spectral saving, however could introduce additional ISI and increased peak variations.

FIG. 10*a* shows a Cross-Correlated (Xcor) embodiment with Gaussian LPF and Integrator as well as sin and cos look-up tables. The TCS outputs of the I and Q baseband signals are further spectrally shaped and limited by sets of I and Q channel filters. A single or multiple cross-correlator (X), cos and/or sin inverter (XCSI) is used in this Agile Cascaded Mis-Matched (MM) (ACM) implementation.

FIG. 11*a* illustrates NRZ signal and shaped Feher Return-to-zero (FRZ) signal patterns and an embodiment having TCS response and cascade LR filters in which the LR filter is implemented with digital IIR and/or FIR filters.

FIG. 12*a* analog implementation components for cross-correlated and/or TCS-filtered data patterns and signals for bit rate agile and for high bit rate applications are shown.

FIG. 12*b* shows an analog BRA baseband implementation alternative of a TCS response processor for cross-correlated or not cross-correlated I and Q signals with selection or combined cascaded LR filter embodiment of this invention.

FIG. 13*a* is a mixed analog and digital circuit implementation alternative of this cross-correlated TCS response processor in cascade with LR filters.

FIG. 14 shows a BRA implementation alternative with a TCS processor, one or more D/A devices in cascade with a bank of switchable LR filters/processors and switchable Linearized Phase or Phase Linear (PL) and Not Linear Phase (NLP) Filters.

FIG. 15 is a detailed implementation diagram alternative of this ACM mode architecture having cross-correlated TCS response wavelet generators in cascade with LR filters.

FIG. 16 shows four (4) illustrative signaling elements generated by analog TCS response cross-correlators, prior to the cascaded LR filters. The shown signaling elements or wavelets are for FQPSK signal generation, having a cross-correlation parameter of A=0.7.

FIG. 17 shows four (4) cross-correlated BRA signaling elements of one of the TCS response analog generated circuits for enhanced performance FGMSK. Only 4 signaling elements are required in this BRA reduced spectrum Feher Gaussian Minimum Shift Keying (FGMSK) signal generation, having a BTb=0.5 parameter.

FIG. 18 shows Differential Encoding (DE) and Differential Decoding (DD) for FQPSK and FGMSK.

FIG. 19 eye diagrams of DE prototype BRA transmit signals for FGMSK with BTb=0.3, and FQPSK with a cross-correlation parameter A=0.7, prior to additional baseband processing and prior to the baseband LR filter of the transmitter are shown. The eye diagram at the TCS response processor output and the I and Q cross-correlated eye diagrams, at the outputs of the cascaded TCS response and LR filters of FQPSK-B systems, operated in ACM mode, as well as the corresponding vector constellation diagrams are also shown.

FIG. 20 shows an FQAM implementation architecture diagram for multi-state Cross-Correlated FQPSK transmitters, also designated as FQAM. In this embodiment a single RF Amplifier operated in fully saturated NLA mode is used.

FIG. 21 is an alternate implementation diagram of multi-state FQPSK, FGMSK and FQAM transmitters. In this embodiment two or more RF amplifiers operated in NLA saturated and/or in partly linearized (LIN) mode of operation are used

FIG. 22 is an "Over the Air Combined" implementation architecture of FQAM signal generation having two or more quadrature FQPSK and/or FGMSK modulators, two or more RF amplifiers and two or more transmit antennas.

FIG. 23 shows the embodiment of an Orthogonal Frequency Division Multiplexed (OFDM) embodiment with FDM signal combining of a number of FQPSK signals. In one of the embodiments of this invention RF Combining is implemented by hardware RF components while in an alternative implementation the RF combining is implemented "over the air".

FIG. 24 shows a transmit Antenna Array and/or RF Combining implementation of multiple modulated signals. This figure illustrates multiple TCS response and/or cascaded TCS response and LR filtered cross-correlated baseband signal processors connected to an antenna array and/or RF combiner.

FIG. 25 shows an ACM and PL architecture and embodiment for trellis coded filtered cross-correlated I and Q baseband signal generation, containing TCS response and cascaded LR filters, for FQPSK, FGMSK as well as FQAM signal generation.

FIG. 26 shows the Power Spectral Density (PSD) of NLA illustrative data links operated at 13 Mb/s rate per link, in the U.S. Government authorized band between 2200 MHz to 2290 MHz. With telemetry standardized filtered PCM/FM 3 links can be used simultaneously, with FQPSK-B the number of links is doubled to 6, while with NLA 16-state FQAM, also designated as a 2^{nd} generation multi-state FQPSK or FQPSK.2.4, the number of 13 Mb/s links is quadrupled to 12 links (over that of standardized PCM/FM).

FIG. 27 The PSD and Integrated Adjacent Channel Interference (ACI) of hardware measured prototype FQPSK-B in a NLA transmitter and of a BRA linearized transmit FQPSK is illustrated in the upper figure. In the lower part of this figure the Integrated ACI of FQPSK systems with that of GMSK (BTb=0.25) systems is compared. For NLA transmitters, the results show a very significant (approximately 2 to 1) RF spectral efficiency advantage of FQPSK over that of GMSK systems. The aforementioned FQPSK 2 to 1 spectral advantage over that of conventional GMSK is measured for a typical −60 dB specification of the ACI.

FIG. 28 Spectral results of 16 state NLA systems are illustrated. The ACI results FQAM, obtained after fully saturated NLA, are compared with that of NLA conventional pre-modulation filtered 16-state QAM systems. The spectral efficiency advantage of the NLA illustrated FQAM is more than 200% over that of NLA prior QAM.

FIG. 29 shows BER performance curves, in terms of the customary BER=f(Eb/No) performance curves, of FQPSK Transceivers. Hardware measurements and/or computer design/software generated data and theoretical study results show that NLA practical RF hardware FQPSK Transceivers, with intentionally and substantially Mis-Matched(MM) filters are within about 0.5 dB to 1 dB of the ideal theoretical LIN amplified QPSK systems.

FIG. 30 shows a demodulation architecture for FQPSK, FGMSK and FQAM and for other signals.

FIG. 31 shows an alternate A/D converter based demodulator architecture. This implementation/embodiment is suitable for "software radio" demodulation and/or for firmware or hardware, or combined hybrid implementations of this invention.

FIG. 32 shows transmit Antenna Arrays (AA) and receive Adaptive Antenna Arrays (AAA) in this multiple transmit and receive omni-directional and/or sectorized or high gain directional antenna-embodiment of this invention. This architecture has the potential to increases the NLA spectral efficiency of FQPSK, FGMSK and FQAM systems to more than 30 b/s/Hz.

FIG. 33 shows a Pseudo-Error (PE)-Non-Redundant Error Detection (NRED) circuit embodiment for on-line or in-service monitor, for PE based adaptive equalization control and for diversity control unit implementations.

FIG. 34 shows an adaptive equalizer circuit embodiment of this invention. The adaptive equalizer, designated as Feher Equalizer (FE) generates the control signals in a PE based NRED circuit and is suitable for fast adaptive equalization.

FIG. 35 is a switchable delay based embodiment of a combined adaptive equalizer/adaptively selectable switched receiver designated as Feher Rake "FR." A PE based NRED or other NRED circuits are used for generating the control and switch selection signals.

FIG. 36 shows an implementation architecture for multiple adaptive FE and FR circuit embodiments with multiple demodulators.

FIG. 37 is a block diagram implementation of a two branch diversity receiver with an adaptive equalizer and a single demodulator. A NRED based circuit generates "smart" diversity selection and/or control signals.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Introductory Description of Embodiments of the Invention

This invention relates in part to Bit Rate Agile (BRA) signal processors and particularly to cross-correlated (abbreviated "CC" or "Xcor") and to Agile Cascaded Mis-Matched (ACM) signal processors for increasing the RF spectral efficiency and RF power efficiency of modulated transmitted signals including digital binary, and digital multilevel signals, and of analog modulated signals operated in linearized (LIN) and in power efficient Non-Linearly Amplified (NLA) systems. Cross-correlated quadrature phase, frequency, and amplitude modulated Transmitter and Receiver (Transceiver) systems are described. The use of section headings is for convenience only and is not intended to delimit the discussion of particular aspects of the invention as aspects, features, embodiments, advantages, and applications are described through the specification and drawings. Acronyms are used extensively throughout the description to avoid excessively long descriptive phrases. In some instances the same acronym is used for a system component or structure as well as as a adjective or other qualifier for the function or operation performed by that structure. The meaning will be clear from the context of the description.

The disclosed BRA systems, designated as belonging to the class of Feher's Quadrature Phase Shift Keying (FQPSK) systems, and also by other acronyms and abbreviations, described herein, include BRA Time Constrained Signal (TCS) response processors and cascaded TCS and BRA Long Response (LR) processors and/or post-processor filters of in-phase (I) and of quadrature (Q) phase signals of BRA transmitters and receivers (or Transceivers when transmitter and receiver are combined). Modulation and demodulation (Modem) Format Selectable (MFS) and Coding Selectable (CS) baseband signal processing implementations and architectures for tunable RF frequency embodiments having Pseudo-Error (PE) based Non-Redundant Error Detection (NRED) implementation structures are also disclosed. BRA demodulation filters Mis-Matched (MM) to that of the modulator filters, filters MM to that of theoretical optimal minimum bandwidth Nyquist filters. PE controlled adaptive equalizers and diversity systems having enhanced spectral efficiency and end-to-end performance are also described and included within the scope of this invention.

In general terms the present invention discloses and provides structure and method for cost effective solutions for Bit Rate Agile (BRA), modulation and demodulation (Modem) Format Selectable (MFS) and Coding Selectable (CS) processors, modulators/demodulators (modems), transmitters and receivers (Transceivers) with agile cascaded mis-matched (ACM) architectures having agile/tunable RF frequency embodiments and which are suitable for power efficient systems. This disclosure contains numerous structural and methodological embodiments and implementation architectures which lead to: (i) significant RF spectral savings, (ii) performance enhancements, and (iii) new features, functions and architectures; none of which were suggested or disclosed in the cited issued patents, inventions and references. Several of the references have been described as 1st generation of Feher's Quadrature Phase Shift Keying (FQPSK), Feher's Quadrature Amplitude Modulation # (FQAM), Feher's Gaussian Minimum Shift Keying (FGMSK), and Feher's Minimum Shift Keying (FMSK) Transceivers.

The new implementation architectures, embodiments and new BRA technologies described in this disclosure are designated as subsets of second generation of FQPSK systems, suitable for BRA operation.

Overview of Exemplary Embodiments Described

A detailed disclosure of implementation architectures and embodiments of this invention is contained in the following sections. In many instances the text is related to the description of the respective figures and to the implementation of ACM transceivers. A changeable amount of cross-correlation between the BRA, CS, MFS and TCS response processor and/or combined or cascaded TCS and LR filters and/or post processor filters of the transmitter with selectable MM between the BRA transmitter and BRA receiver and CS processors, including single and separate in-phase (I) and quadrature (Q) signal storage/readout generators and single and/or separate I channel and Q channel D/A architectures for cross-correlated BRA, MFS and CS formats are also described. In agile cascaded mis-matched (ACM) designs for NLA and for Linearized (LIN) amplifiers selectable FQPSK filtering strategies, in the transmitter and separately in the receiver lead to further improvements in spectral efficiency.

Within an interface unit (IU) **107** in FIG. **1***a* a generalized block diagram of an embodiment of this inventive Transceiver **100** is shown and includes a BRA **102**, MFS, CS, MM filtered and RF frequency agile enhanced spectral efficiency, high performance Transceiver block diagram. In this embodiment one or more input signals **150-1**, **150-2**, . . . , **150-N** are received on single or multiple lead(s) **101-1**, **101-2**, . . . , **101-N** and provided to a transmit section **152** of Interface Unit (IU) **102**. The term lead or leads generally refers to a coupling or connection between the elements, and

may for example refer to a wire, integrated circuit trace, printed circuit trace, or other signal link, connection, or coupling structure or means as are known in the art. Note that the IU provides an Interface port for transmission, designated as **102** and in the Receive section, also designated as **102**, it contains the required IU receive processors and provides an output interface port. The input and output leads may contain and communicate analog or digitized voice, music, data, video, telemetry or other signals, or combinations thereof. In the FIG. **1***a* embodiment, signals **150** on input leads **101** may also represent Spread Spectrum, CDMA, WCDMA, CSMA, TDMA, FDMA or continuous single channel "Clear Mode", or other signals such as FDM and orthogonally frequency division multiplexed Orthogonally Frequency Division Multiplexed (OFDM) signals and IU port configurations.

The BRA **102** unit, shown in FIG. **1***a* provides signals **153** to a Base-Band Processor (BBP) unit **103**. This unit **103**, receives in addition to the output signals from the IU **102**, signals on lead **104** a Clock (C), on lead **105** one or more Control (CTL) signals and on lead **106** one or more Sampling (SAM) signals. The combination of the aforementioned C, CTL and SAM signals is also designated with a common further abbreviation as "C".

BBP unit **103** provides a new class of BRA Cross-Correlated (CC) signals, including ACM filtered signals. The BBP provides signals to the Quadrature Modulator (QM) unit **109**. Numerous embodiments of QM **109** have been described in the prior art and/or in the listed references. The QM implementation in baseband, IF and RF frequency ranges is well known by means of analog, digital and combined analog or digital techniques in hardware, firmware and in software and does not require further description. The Frequency Synthesizer, Unit **108**, provides one or more unmodulated "Carrier Wave" signal(s) to the QM. The quadrature-modulated signals are provided to the Transmit Amplifier (AMP). The amplifier may be operated in a fully saturated mode, designated as Non-Linear Amplifier (NLA) or C-class amplifier or it may be operated in a Linearized (LIN or Lin) mode. Between the QM-**109** and the Transmit AMP **111** part of the "RF Head" an optional combiner **110** is shown. Combiners **110** and/or post-AMP combiner **111** are optional units for Pilot Insert (PI) **1** and **2** designated as units **109** and **112**, respectively. The RF head's transmit AMP is connected to Switch (SW) and/or Combiner/Splitter device **113** and this **113** unit provides the signal for transmission to and from antenna **114**. Instead of the aforementioned antenna a separate port could be used for signal transmission or reception of "wired" systems. The Pilot Insert (PI) optional units may provide in band/or out of band pilot tones for transmission. These tones could be used for fast and robust performance receiver demodulators and synchronizers. In the transmit and receive sections Switch **113** or Switch or Combiner or Diplexer is connected to the receive Band Pass Filter (BPF) **115**. Instead of Switch **113** a Combiner/Splitter could be used. The received signal after the BPF is connected to a Low Noise Amplifier (LNA) unit **116**. The optional down-converter unit **117** receives its inputs from the Frequency Synthesizer and from the LNA and provides it to band-pass filter (BPF) **118** for further processing. The entire down-conversion stage of the receiver, including the receive section of the Frequency Synthesizer, mixers **117** and **118** are deleted for the so-called Direct Down-Conversion type of receivers.

The quadrature demodulator (Quad Demod) may contain components such as Automatic Gain Control (AGC), Frequency Tracking, Synchronization and Post Demodulation, Signal Conditioning including Symbol Timing Recovery (STR) circuits. The demodulated signal provided by demodulator unit **119** is fed to the receive section of the IU **102**. The receiver section of the IU **102** contains on lead **101** the output signal and output port.

In FIG. **1***b*, an alternate, somewhat generic Transmitter (Tx) block-implementation diagram of this invention for Bit Rate Agile (BRA), Modulation Format Selectable (MFS) hardware, firmware and/or software implementations, including optional single and multi-tone inserts at one or more locations and optional ACM embodiments, is depicted. Several optional interface units prior to the processor unit **132** are illustrated in this figure. These units may perform the transmit interface functions and the corresponding receive interface functions. Illustrative examples for the transmit interface functions are described. Unit **120** illustrates a Forward Error Correction (FEC) and/or a Differential Encoder (DE). Unit **121** is an interface for Frequency Division Multiplexing (FDM); for Collision Sense Multiple Access (CSMA) **122** would be used.

For Code Division Multiplexes (CDMA) and its variations such as W-CDMA and B-CDMA and 3rd generation CDMA **123** would be used. For time division multiplexed (TDM) **124**, while for Continuous single or multiple digital or analog signals or Analog to Digital (A/D) converted signals unit **125** is used. For Telemetry interface **126**, while for Broadcast Signal interface **127** is used. Unit **128** is suitable for Orthogonal Frequency Division Multiplexing (OFDM). For additional CDMA processing or interface **129** could be used. Trellis Coded Modulation (TCM) baseband processing of the trellis encoder and corresponding optimal demodulation/decoding could be performed in **130**. Unit **131** is reserved for "other" emerging applications. Unit **132** is the processor, including the BBP for a generic class of signal generators disclosed in this invention. The baseband "in-phase" (I) and quadrature phase (Q) baseband signals generated by **132** are provided to QM **133**. The QM unit receives an input also from the Carrier Wave (CW) generator also designated as Local Oscillator (LO) which could be part of the Frequency Synthesizer (FS) **140**. The quadrature modulated output signal in one of the optional embodiments is combined with one or more Pilot Tones in combiners **134** and/or **136**. Signal Amplifier (AMP) **135** provides the amplified signal to the Transmit and Receive Antenna **138** through switch or combiner/splitter **137**. For wired applications such as telephony, coaxial cable, fiber and other physical wired connections interface unit/amplifier **139** is used. Bit Rate Agile Clocks (BRAC) are generated and/or processed in **141**. The Control (CTL) signals are obtained from unit **142** while one or multiple rate or sub bit rate Sampling Signals (SAM) are generated and/or processed by **143**.

In FIG. **2** an embodiment of a BRA integrated Base-Band Processor (BBP) with BRA post filters and BRA Cross-Correlated (CC) signals and ACM filters for quadrature modulation is illustrated. New BRA, MFS, CS and RF frequency agile implementation architectures of this invention are described in conjunction with FIG. **2**. On signal leads **2.10** and **2.11** the in-phase input (Iin) and the quadrature phase input (Qin) signals are provided to switch units **2.14** and **2.15**. On lead **2.12** a serial input signal (Sin) is illustrated. This signal is connected to a Serial-to-Parallel (S/P) converter and/or Splitter unit, combined or individually also designated as "splitter" **2.13**. Switching and/or combining units **2.14** and **2.15** provide in-phase (I) and quadrature phase (Q) baseband signals to the BRA processor **2.16**. This BRA processor also receives a set of Clock, Control, and Sampling Signals C, CTL and SAM, com-

monly also referred to as set of C signals or merely "C" signal or "C" for clock. The Iout and Qout signals are on leads 2.17 and 2.18 and provide inputs to the QM. The QM 2.19 provides drive signal (S) to amplifier 2.20 which in turn provides amplified signals to switch or combiner/splitter unit 2.21. Antenna 2.22 and/or interface port/amplifier 2.23 provide the signal to the transmission medium. Unit 2.19 Frequency Synthesizer (FS) provides the Carrier Wave Signals to one of the inputs of the QM and may provide one or more pilot tones to the QM and/or the output of 2.20 for combining the pilot tone(s) with the quadrature modulated signal.

In an alternative implementation of the baseband processor, in the lower part of FIG. 2, on leads 2.24 and 2.25 parallel input signals (Iparin) and (Qparin) are provided, while on lead 2.26 a serial input signal is provided. Units 2.27, 2.29, 2.30, 2.32, and 2.33 are switching devices for the serial signal input and for the I and Q signals. Unit 2.28 represents a signal splitter. Signals and units 2.10 to 2.33 constitute some of signal processing components of this new architecture. These components have related structures to the description contained in Feher's prior art U.S. Pat. No. 5,491,457, Ref. [P2]. However, significant structural and implementation differences exist between the structures described in [P2] and the entire structure and embodiment of FIG. 2.

The architecture and embodiment of the Bit Rate Agile embodiment of the FIG. 2 processor includes BRA Baseband Processor (BBP) 2.34 with cascaded BRA Time Constrained Signal (TCS) response and Long Response (LR) signal generators. BRA post filters with Cross-Correlated (X) Cosine (C) and Sine (S) single or multiple processors and inverters (XCSI) are also part of the new structure. These structures, devices and architecture, including the new ACM filtering features available with these new elements are part of this invention.

Description of an Exemplary Embodiment of a FQPSK Bit Rate Agile Transceiver

In this part of the detailed description of the invention the focus is on Quadrature Modulated (QM) four (4) state FQPSK systems. These four state systems have in general, in the sampling instants, in the I and Q baseband channels 2 signaling states (for short "states"). In the baseband I channel and in the baseband Q channel there are 2 signal states. The architectures and embodiments of nine (9) state FQPSK systems are essentially the same as that of 4 state FQPSK Transceivers. An exception is that the baseband I and Q Cross-Correlated and BRA signal processors provide 3 level (state) baseband I and Q signals and results in 3x3=9 state modulated FQPSK systems. Most implementations and embodiments and alternatives apply to multi-state (more than 4 state) Quadrature Modulated systems, described in later sections, such 9, 16 or 64 or 256 state QM systems having 3, 4, 7, 8 and 16 states in their respective baseband channels.

FIG. 3 shows BRA baseband filters and processors preceded by a "basic cross-correlator (Xcor)" component of this FIG. 3. The basic Xcor component, including the wavelet storage units and multiplexers may be related to implementations described in the prior art Kato/Feher U.S. Pat. No. 4,567,602 patent [P5]. In some of the implementations of the present BRA invention, for use in BRA post filtered/processed system applications, these basic Xcor elements are used with integrated and/or post Xcor BRA filtered/processed ACM units. In some other embodiments different basic signaling elements including cascaded Time Constrained Signal (TCS) response and Long Response (LR) waveform generators and BRA post filters are used. In alternate embodiments of this invention the basic Xcor is connected to Cross-Correlated (X) Cosine (C) and Sine (S) single Inverters (XCSI). In some other alternate implementations the basic Xcor unit is not used. The combined embodiment and structure of the set of TCS and BCM signal generators, collectively designated as unit 3.11, combined with Multiplexers 3.13 and 3.14 and cascaded with the BRA cascaded TCS response and LR filters and baseband post filters 3.15 is different from that of the aforementioned prior art [P5].

FIG. 4 shows a trellis coded processor implementation architecture. Variations of this structure include one or more elements illustrated in FIG. 4. The shown structure is suitable for encoded signal generation including Differentially Encoded (DE) and/or Non-Redundant Trellis Coding (TC) of the Baseband Processed filtered I and Q signals. Alternately other Forward Error Correcting (FEC) devices are contained in unit 4.13. The architecture of this FIG. 4 is suitable for several 2^{nd} generation FQPSK embodiments. Elements of this structure generate enhanced spectral efficiency LIN and NLA constant envelope and non-constant envelope systems. BRA digital and analog implementations of ACM selectable parameter cross-correlators and several sets of transmit and selectable receive filters are included. Synchronous single data stream and asynchronous multiple data stream input processing has been also implemented with the shown structure of FIG. 4. Transmitters with and without preambles and trellis or other encoders and/or analog and digital pilot insertion as well as multi-amplitude cross-correlated signals including 3 level 7 level and multi-level partial response signals are also generated with the "mix and match" flexible and interoperable elements and structures.

On leads 4.11 and 4.12 the in-phase and quadrature phase input signals Iin and Qin are illustrated. Units 4.13 and 4.14 contain Digital Signal Processors (DSP) or FPGA logic elements, or other readily available processors. These processors perform functions such as Trellis Coding (TC) with or without redundancy, Differential Encoding (DE), Digital Signal Mapping for TC or other logic and/or memory modifications of the baseband signals. The Digital Processing Addition (DPA) unit 4.15 is provided for additional optional DE, Digital Pilot Insertion, and addition of Forward Error Correction (FEC) bits and/or symbols, including CRC and/or pi/4 rotation of the QM signal. Element 4.16 is a Bit Rate Agile (BRA) Base-Band Processor (BBP) which includes post-BBP ACM filters and/or post-Cross-Correlation (CC) filters and processors in the I and Q channels or a shared filter for the I and Q channels. The aforementioned functions and implementations could be used in the described sequence, or in a permutation or combination or variation of the aforementioned sequence. The entire processor of FIG. 4 could be implemented in one or more integrated steps without specific separation of the aforementioned functionality and/or implementation architectures.

One of the implementation alternatives of the Differential Encoded (DE) algorithm, used in some of the embodiments of this invention is described in the following paragraphs. In FIG. 4 the optional DE is part of unit 4.13 and is used for FQPSK and in particular for a specific FQPSK embodiment, designated as FQPSK-B, Revision A1 as well as FGMSK, FMSK and FQAM Transceivers. A somewhat more detailed implementation block diagram of entire Differential Encoder (DE)-Differential Decoder (DD) and corresponding Serial to Parallel (S/P) and Parallel to Serial (P/S) converters is shown in FIG. 18.

A Serial-to-Parallel (S/P) processor, such as processor 18.1 of FIG. 18, is inserted prior to the DE 4.13 of FIG. 4 or prior to the DE unit 18.2 of FIG. 18. The Differential Encoder 4.13 Differentially Encodes (DE) the I and Q data streams. The baseband I and Q signals are differentially encoded as follows:

$$I=D_{even}\oplus Q^{bar}$$

$$Q=D_{odd}\oplus I$$

In an alternative implementation of the aforementioned DE the inversion "bar" is on I in the second equation instead of the Q of the first equation (that is I-bar rather than Q-bar).

$$I=D_{even}\oplus Q$$

$$Q=D_{odd}\oplus I^{bar}$$

In one of the FQPSK embodiments, designated as FQPSK-B, one of the implementations has the I and Q data symbols offset by one bit time (Tb), corresponding to a ½ symbol time (Ts), i.e. Tb=Ts/2. D_{even} and D_{odd} are the even and odd input data bits. In alternate embodiments, the aforementioned offset is not used. In the case of Direct Sequence Spread Spectrum systems such as certain CDMA systems, instead of the offset by 1 bit time the offset could correspond to 1 chip time or to a presetable time.

In FIG. 5 several Time Constrained Signal(TCS) response patterns are illustrated. TCS and/or TCS response patterns are illustrated, described and defined with the aid of the synonymous terms "Signaling Elements(SE)", "Signal Components" or "Wavelets." The terms TCS, TCS processor and/or TCS response shall mean that the pulse response or alternatively the impulse response of TCS processors is constrained to the length of the memory of TCS processors. This TCS response may have an impact on the cascaded response of a TCS processor with that of subsequent filters. TCS response cross-correlated and also TCS response signal patterns without cross-correlation are illustrated in FIG. 5. These are used in some of the implementations of this invention as signaling elements or wavelets connected in cascade to Long Response (LR) filters. The term "Long Response filter" or "LR filter" means that the measurable pulse response and/or impulse response of an LR filter or processor is longer than the pulse response of the TCS response processor. In several implementations the LR filter is implemented by conventional filter synthesis and design. Conventional filter designs include the design and implementation of active and passive Bessel, Butterworth, Chebycheff, Gaussian, analog and digital filters and of hybrid analog/digital filters. In alternate LR filter designs Infinite Impulse Response (IIR) and also Finite Impulse Response (FIR) architectures are implemented.

The pulse response of TCS response processors is limited to the memory of the TCS processor. In several embodiments the memory of the TCS processor and/or TCS cross-correlator has been between ½ and 3 symbol duration Ts intervals. The pulse response of LR filters is related to the type of the selected filter, the roll-off and the 3-dB bandwidth(B) and bit rate duration (Tb). For example an 8^{th} order Chebycheff filter, having a BTb=0.5 could have a practical, measurable pulse response of more than 10 bit duration. A 4^{th} order Butterworth filter having a BTb=1 could have a practical pulse response of more than 4 bit duration, depending on the accuracy/inaccuracy of pulse response and resulting Intersymbol Interference (ISI) definitions and requirements.

The basic TCS signaling elements or "Wavelets" shown in FIG. 5 precede the LR filters of the ACM embodiments. In alternate architectures the sequence of TCS and of the. LR filters/processors is interchanged and also used in parallel architectures for combined TCS and LR signal generation. The TCS signal elements or for short "Signals" or "wavelets" in FIG. 5 are described as follows: signal pattern 5.11 represents pattern S1(t) of a Non-Return-to-Zero (NRZ) signal pattern. The NRZ signal pattern contains TCS signaling elements where the duration of each NRZ signaling element is constrained to one Time Symbol (Ts) duration. Signal pattern 5.12, also designated as S2(t), represents an other one Time Symbol TCS response wavelet pattern. This TCS response signal could be generated by the "Superposed Quadrature Modulated Baseband Signal Processor" (SQAM) Seo/Feher's U.S. Pat. No. 4,644,565, Ref. [P4]. Another TCS pattern, designated as pure Intersymbol-Interference and Jitter Free (IJF) signal pattern, or pure IJF wavelet and pattern, based on Feher's U.S. Pat. No. 4,339,724 [P7] is signal 5.14 also designated as S4(t). It is a TCS pure IJF signal pattern corresponding to the alternate NRZ pattern example shown as signal 5.13 and designated as S3(t). Signals 5.15 and 5.16 designated as S5(t) and as S6(t) are in-phase (I) and quadrature phase (Q) half a Time Symbol (Ts) time delayed NRZ baseband signals. In this designation half a symbol duration corresponds to one Time Bit (Th) duration that is Ts=Tb/2. Signal patterns 5.17 and 5.18 corresponding to S7(t) and as S8(t) are additional illustrative examples of TCS signals. These TCS signals represent in-phase(I) and Quadrature-phase (Q) baseband Cross-Correlated (CC) or (Xcor) signal patterns which could be generated by use of the Kato/Feher U.S. Pat. No. 4,567,602, Ref. [P5]. These S7(t) and S8(t) cross-correlated TCS response signal patterns represent IJF encoded output signals having amplitudes modified from the peak amplitudes of IJF signals.

In FIG. 6 an implementation diagram with cascaded switched transmit (Tx) and receive (Rx) Low-Pass-Filters (LPF) in conjunction with cross-correlated and other non cross-correlated TCS response and cascaded LR processors is shown. These LR processors could be implemented as separate I and Q LPF s or as an individual time-shared LPF. The Transmit Baseband Signal Processor (BBP) including the I and Q LPFs could be implemented by digital techniques and followed by D/A converters or by means of analog implementations or a mixture of digital and analog components. External Clock and External Data Signals are used to drive the S/P and the entire baseband processor (BBP). The BBP may include a Differential Encoder (DE). The I and Q LPFs may be implemented as single filters (instead of cascaded filters). Modulation and Demodulation filters have been implemented and tested with intentionally Mis-Matched (MM) filter parameters. Some of the best performance implementations use Agile Cascaded Mis-Matched (ACM) architectures. LR filters have been synthesized and implemented as phase equalized and also as non-equalized phase response transmit and receive Bessel, Gaussian, Butterworth and Chebycheff filters. Bessel, Gaussian and Butterworth and Chebycheff filters as well as other classical filters are within the previously described and defined class of Long Response (LR) filters. These filters have a relatively long practical impulse and/or pulse response. The measurable practical pulse response of the aforementioned filters having an approximately BTs=0.5 design parameter extend to many bit durations. Here B refers to the 3 dB cut-off frequency of the filter and Ts to the unit symbol duration. From classical communications and Nyquist transmission theory it is well known that the theoretical optimal performance minimum signal bandwidth is

defined for BTs=0.5. The LPFs in the I and Q channels, or the shared single set of LPFs, implementations include Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) filters.

In FIG. **6** on lead **6.3** a serial data stream is present. This signal is provided to **6.4***a* and the optional **6.4***b* units for Serial-to-Parallel (S/P) conversion and a 1 bit duration (Tb) offset in one of the implementations. In other implementations there is no offset delay **6.4***b* in the embodiment. Some other alternate embodiments use a selectable offset delay **6.4***b* which is larger or equal to zero and smaller than the duration of approximately 200 bits. As stated the Offset logic is used in certain embodiments, while in other architectures it is not present. The input signal or input signals are provided on leads **6.1** and **6.2** instead of lead **6.3** in some of the alternative implementations of this invention. Unit **6.5** is a Base-Band Processor. Unit **6.5** may be clocked, controlled and sampled by signals such as C, CTL, and SAMP such as illustrated previously in FIG. **1** to FIG. **3**. In this figure, FIG. **6**, all of these clocking, control and sampling signals which could represent multiple rates and multiple leads are collectively or individually abbreviated simply as "C" and illustrated with an arrow near the letter "C." Unit **6.5** in some of the embodiments performs the Time Constrained Signal (TCS) processing, waveform assembly and generation functions of multiple symbol TCS cross correlation and signal processing operations. The I and Q outputs of unit **6.5** are provided as inputs to the transmit set of LPFs designated as TX1 LPF-1 unit **6.6** and TXQ LPF-1 unit **6.11**. This set of first LPFs could be cascaded with a second set of I and Q channel LPFs units **6.7** and **6.13**. Switch units **6.8** and **6.12** illustrate that the second set of LPFs could be bypassed and/or deleted in some of the embodiments.

The LR filter units, embodied by the first and second sets of I and Q are implemented as LPFs or alternately as of other types of filters such as Band-Pass Filters (BPF) or High Pass Filters (HPF) or other filter/processor LR filter combinations. As stated previously, for several embodiments all of the aforementioned processors are BRA and ACM, while for other implementations bit rate agility and/or ACM may not be required. Units **6.9**, **6.10**, **6.14**, **6.15** and **6.16** comprise a quadrature modulator in which the I and Q modulators are 90-degree phase shifted and in which a Local Oscillator (LO) is used as a Carrier Wave (CW) generator. Unit **6.17** is an amplifier that could be operated in a LIN or in a NLA mode. The output of amplifier **6.17** is provided on lead **6.18** to the transmission medium.

In FIG. **6** at the receiving end, on lead **6.19**, is the received modulated signal. Unit **6.21** is a BPF that is present in some embodiments while in others it is not required. Alternatively the receive BPF could be "switched-in" or "switched-out" by switch **6.20**. In some implementations Surface Acoustic Wave (SAW) BBF were used to implement **6.21**. Units **6.22**, **6.23**, **6.24** and **6.25** embody a Quadrature Demodulator (QD) with a corresponding Local Oscillator (LO). The aforementioned LO represents for some embodiments an entire Carrier Recovery (CR) subsystem while for other embodiments it is a free running LO. The set of LPFs **6.26** and **6.27** are the embodiment of post-demodulation filters, while the second set of LPFs **6.28** and **6.29** may be used to further enhance the spectral efficiency advantages or other performance advantages of designed ACM systems. The second set of LPFs could be connected or disconnected by switches **6.30** and **6.31** or entirely deleted. Unit **6.32** is the Clock Recovery (CR) and/or Symbol Timing Recovery (STR) system. For fast clock and/or STR, this unit is connected in some of the embodiments in parallel to the Carrier Recovery (CR) subsystem. In one of the embodiments of fast Clock Recovery (CR) systems, the parallel configuration embodied by units **6.37** and **6.38** is used for discrete signal clock generation. The discrete signal spike, in the frequency domain, provides on lead **6.39** the clock recovery unit **6.32** with a discrete spectral line signal which is exactly at the symbol rate or at the bit rate. In this architecture unit **6.37** is a multiplier or any other nonlinear device which has at its input the received modulated signal and the same received modulated signal multiplied by a delayed replica of itself. The aforementioned delayed replica is generated by unit **6.38**, a delay element. The receiver structure, shown in FIG. **6**, is one of the many possible alternative receiver and demodulator structures. It is interoperable compatible and suitable for BRA and MFS and CS reception, demodulation and/or decoding of the transmitted signals embodied by means of the BRA and/or MFS and/or CS and/or ACM implementation of the FIG. **6** transmitter embodiments.

Contrary to the teachings and wisdom of well established bandwidth efficient communication theory, of matched filter-optimal demodulation theory and optimal data reception theories, in several embodiments of the current invention, substantially Mis-Matched (MM) modulator and the demodulator filters have been implemented. Fundamental and pioneering discoveries, regarding the cascaded pulse response of TCS response and of LR filter cross-correlated BRA implementations of modulator I and Q filters and that of the implementations of "matched " and/or intentionally "Mis-Matched" (MM) demodulator filters are disclosed in this part of the invention. In classical communication theory the demodulation LPFs, and in fact the entire cascaded receiver and demodulation filter responses are matched to the characteristics of the modulator and entire cascaded modulator and RF transmitter filters. Minimum bandwidth-maximal spectral efficiency, optimal performance requires that the Nyquist minimum bandwidth theorems be satisfied for ISI free and matched signal transmission/reception. The intentionally and substantially Mis-Matched (MM) transmit and receive filter designs, used in implementations of this invention lead to simpler implementations than implied by communication matched filter theory and by Nyquist minimum bandwidth theories and to substantially improved performance for RF power efficient NLA transceivers. From communications theory, numerous books, referenced publications as well as from patents it is well known that for "optimum" performance the cascaded filters of the modulator should be matched by the cascaded receive demodulator filters. For example, in a conventional bandlimited QPSK system, if Nyquist filters are implemented as "raised cosine filters", then the best "optimal" performance is attained if the cascaded transmit and receive filters have a raised cosine transfer function and the filtering is equally split, i.e. "matched "between the transmitter and receiver. For pulse transmission, such as filtered NRZ data an aperture equalizer, having an wTs/sin(wTs) frequency response is used in theoretical optimal transmitters, prior to the implementation of the transmit matched filter. Specifically, based on Nyquist transmission and filter theories, combined with matched filter receiver theories the 3 dB cut-off frequency of an optimal minimum bandwidth transmit filter, used as a baseband I or Q channel filter, in a QPSK system equals ½ of the symbol rate or alternatively ¼ of the bit rate. The 3 dB bandwidths of the modulator and demodulator filters of the "theoretical optimal" bandlimited QPSK system are matched. The 3 dB bandwidth of the theoretical optimal system it is the same for the modulator filter and for the

demodulator filter. If these filters are implemented by pre-modulation LPFs and post-demodulation LPFs then the aforementioned theoretical bandwidth corresponds to BTs=0.5. This value corresponds to BTb=0.25, where B is the 3 dB bandwidth of the respective filters, Ts is the unit symbol duration and Tb is the unit bit duration.

Contrary to the teachings of the aforementioned optimal performance matched filter modulation demodulation theory, we disclose the implementation of demodulator architectures and embodiments with "Mis-Matched" (MM) filtering, and specifically for agile (bit rate) cascaded mis-matched (ACM) implementations. The term Mis-Match (MM) refers to intentional and substantial MM between the cascaded 3 dB bandwidth of the I and Q demodulator filters and/or to the MM with respect to the Nyquist theory stipulated bandwidth, with that of the cascaded response of the modulator I and Q filters. Alternate embodiments include MM pre-modulation baseband LPF and post-demodulation baseband LPF designs as well as post modulation BPF transmitter implementations and receiver pre-demodulation BPF implementations. A combination of the aforementioned baseband and BPF designs has been also implemented. The term "substantial" MM in a BRA architectures and embodiments such as shown in the alternate implementation diagrams in FIG. **6** or FIG. **7** or FIG. **10** to FIG. **15** and/or FIG. **25** or FIG. **30** implies typically more than about 30% mis-match between the respective 3 dB cut-off frequencies of the transmit and receive filters, but this value is exemplary and is not a limiting amount of mis-match.

One of the best known BRA implementations of FQPSK systems is designated as the "FQPSK-B" family of transceivers. In this section, several best embodiments of FQPSK-B Transceivers, operated in NLA systems are described. The implementation of the FQPSK-B embodiment, described in this section has BRA, CS and MFS architecture with substantially MM modulation and demodulation filters. The modulator TCS response processors cascaded with the LR filters and the demodulation filters are Mis-matched (MM). In this FQPSK-B implementation a cross-correlation factor of A=0.7 has been implemented between the I and Q baseband TCS response processors which are cascaded with the LR filters. The TCS wavelets and assembly of the TCS wavelets has been described in the Kato/Feher patent Ref. [P5]. A resulting I and Q cross-correlated data pattern of this implementation, at the TCS processor output and prior to the BRA LR filters is shown in FIG. **5** as TCS data patterns S7(t) and S8(t) having a cross-correlation parameter A=0.7. The I and Q baseband signal patterns are generated with several structures and elements, described as parts of this invention. The aforementioned TCS signal patterns are available at the outputs of the following elements: in FIG. **6** at the output leads of TCS **6.5**, in FIG. **7** at the output leads of D/A Units **7.8** and **7.11**. In FIG. **8** at the output leads of units **8.7** and **8.8**. In FIG. **10***b* at the output leads of the D/A converter units **10***b*.**17** and **10***b*.**18**, and in FIG. **15** at the output leads of D/A converter (designated as DAC's) units **15.7** and **15.14**.

The aforementioned BRA, MFS, CS and intentional Mis-matched (MM) implementations and embodiments of four state FQPSK Transceivers, operated over NLA systems are applicable to Multi-State NLA systems, described in later sections.

In FIG. **7** one of the alternate implementations of Bit Rate Agile (BRA) transmitters is shown. The illustrated embodiment of the current invention uses a variation and alternative implementations of the "Basic Cross-Correlator" (XCor) and post cross-correlation processors, as disclosed in prior patents of Feher et al., with several original embodiments described in conjunction with FIG. **7**. In cascade with the basic Xcor which implements TCS response processed cross-correlated or TCS not-cross-correlated signals is a second set of LR filtered processors. In cascade with the 2nd processor and with Digital to Analog (D/A) converters are pulse shaping bit rate agile LR filters, implemented as Low-Pass-Filters (LPF) or other type of filters in the I and Q channels. As stated previously, BPFs, HPFs or other types of processors/filters could replace the LPFs. On lead **7.1** is the input signal to unit **7.2**, which implements S/P, DE and Gray encoding and/or other logic functions. Logic **7.3** is a cross correlator that is used to cross correlate I and Q signals. The duration of the cross correlation processor and implementation of the basic Xcor is selectable in the current invention. It is selectable in a wide range, from zero, i.e. no cross-correlation to a fraction of a bit interval, and is adjustable and/or selectable up to many bits and/or symbols. In some of the alternate implementations of FIG. **7** the entire cross-correlation Unit **7.3** designated as "Logic" is not used, that is, it is deleted from FIG. **7**, in the generation and assembly of the TCS response signals, provided by the signal generator set **7.4**. In logic/cross-correlator **7.3** six symbol shift registers are shown for the I and Q channels. As stated in alternative embodiments the cross correlation is deleted. The basic signaling elements, also referred to as wavelets, designated F1, F2, . . . , F16 are generated and/or stored by a set of signal generators or storage devices designated as **7.4**. The aforementioned storage units or wavelet generators are implemented in one of the alternate embodiments with ROM and/or RAM chip sets and/or are part of a firmware and/or software program. In certain embodiments a fairly large number of wavelets are generated, i.e., a set of S0, S1, S2, . . . , S63 or even more wavelets are generated, while in other embodiments only 2 or 4 signaling elements (wavelets) are used. In alternate implementations instead of generating and/or storing separate and distinct signals or "wavelets", a very small number of wavelets is stored and their inversions in terms of amplitude inversion and time inversions are used. In the embodiments of the current invention the elements are suitable for BRA and ACM operation. Units **7.5** and **7.6** are designated as two multiplexes and are embodied in some implementations as a single integrated multiplexer unit or more than one unit. In one of the embodiments all digital processors, including units **7.2** to **7.16** are implemented as a single fiction and unit. Unit **7.7** is a second processor and provides for optional additional cross correlation and amplitude limiting, also designated as signal clipping or Peak Limiter(PL). PL are implemented by clipping devices and/or other commercially available prior art nonlinear devices. Other conventional devices described previously in these specifications as well as in the prior art literature embody units **7.8** to **7.13**. Amplifier **7.15** provides the RF modulated signal to the antenna **7.17** through a switch and/or combiner or splitter **7.16**.

In FIG. **8** a Quadrature Modulated (QM) Transceiver embodiment of this invention is shown. On lead **8.1** the input signal is provided to the optional S/P and/or DE and/or Logic/Coding processor **8.2***a*. Unit **8.2***b* is an optional (Opt.) Xcor, designated in FIG. **8** as Xcor 1. Unit **8.2***b* provides I and Q signals through the optional offset delay, D1 unit **8.3** or optional bypass switch **8.4** for further processing to units **8.5** and **8.6**. Units **8.5** and **8.6** implement one or more I and Q processing operations of Intersymbol Interference(ISI) and Jitter Free (IJF) signals such as cross-correlated

amplitude-adjusted IJF signals or other TCS cross-correlated and/or non-cross-correlated signals including binary and multilevel SQAM signaling elements in cascade with LR filter subsystems such as IIR and/or FIR processors which are operated in a BRA mode. Units **8.7** and **8.8** are D/A optional single shared D/A, or multiple D/A converters that provide signals to the second set of filters **8.9** and **8.10**. Analog, digital or hybrid hardware, software or firmware in unit **8.11** implements an optional cross correlator. The I and Q output signals of **8.11** are provided as baseband drive signals of the QM **8.12**. Local Oscillator (LO) **8.13** provides the RF unmodulated CW to the QM. The QM provides to Amplifier **8.14** a signal for amplification to antenna **8.15** or to the transmission medium. One of the embodiments has a very simple/efficient implementation of the TCS response cross correlated transmit (Tx) processor with only 4 samples/symbol and only three(3) wavelets.

In FIG. **9** Peak Limited (PL) and other TCS response signal patterns of this invention as well as that generated by the prior art Superposed Quadrature Modulated Baseband Signal Processor ("SQAM") Seo/Feher's U.S. Pat. No. 4,644,565, Ref. [P4] are illustrated. Signal pattern designated as **9.11** is a conventional prior art NRZ signal, while TCS pattern **9.12**, if it is not cross-correlated with an other signal or not cascaded with a LR processor, represents a processed prior art SQAM generated baseband signal wavelet pattern. If the TCS pattern **9.12** signal is connected to BRA one or more filters, including LR filters and/or ACM Processor's and it is part of I and Q cross-correlated signal generators and BRA processors, then it is a new implementation of this invention, having a substantially enhanced bandwidth efficient signal. Signal pattern **9.12** is reproduced as signal pattern **9.13**. The dotted line of signal pattern. **9.14** illustrates the TCS processor and cascaded Long Response (LR) filtered output sample signal pattern. The **9.14** LR filtered signal pattern is more spectrally efficient than the **9.12** TCS response signal, however it may contain more Intersymbol-Interference (ISI), more Data Transition Jitter (for short "Jitter") and higher signal peaks than the TCS signal pattern. A PL or "Clipped" signal pattern **9.16** of this invention is illustrated with dotted lines adjacent to signal pattern **9.15**. Signal clipping and/or smooth gradual or soft PL or abrupt peak limiting of TCS, and/or of TCS response processors cascaded with LR filters and/or cross-correlated signals reduces the overall signal excursion of the peak to peak amplitude variation of the I and Q signals. It also reduces the envelope fluctuation of the I and Q modulated signal. Applications include I and Q analog and digital signals, including Orthogonal Frequency Division Multiplexed (OFDM), clear mode non-spread spectrum as well as spread spectrum signals, such as CDMA and also TDM or TDMA, CSMA and FDMA architectures.

A Cross-Correlated (Xcor) embodiment of this invention for a BRA architecture, and also suitable for ACM operation, is shown in FIG. **10***a*. It is suitable for several classes of FQPSK, FMOD, FGMSK, FMSK, FGFSK and FQAM implementations. The implementation includes Gaussian LPF and Integrator and/or other filter processor as well as sin and cos look-up and/or other "look up tables". BRA implementations and implementation of TCS and LR filtered/processed Cross-Correlated (CC) baseband I and Q signals and the corresponding Quadrature Modulator (QM) and RF amplifier (Amp) are included in the embodiment of FIG. **10***a*. The aforementioned term "look up tables" refers to TCS response wavelet storage and/or wavelet generation units. In alternate embodiments the sin and cos wavelet generators and/or wavelet storage and readout units are replaced with other wavelets than the aforementioned sin and cos function generated wavelets. On lead **10***a*.1 an input analog, digital or mixed signal is provided to Unit **10***a*.2 also designated as Filter **1**. This filter as well as other components of the transmitter are Clocked/Controlled and/or Sampled by one or more **10***a*.3 signals, designated for short by the letter C. Filter **1**, **10***a*.2 is a Gaussian shaped, Butterworth, Bessel or other filter or combination of filters and processors and it is configured in LPF, BPF or HPF mode. Unit **10***a*.4 is a second signal processor. It embodies an Integrator or some TCS signal shaping units and/or LR filter ACM implementation. Splitter **10***a*.5 splits the signal into I and Q signals and it may implement the splitter and/or Serial to Parallel (S/P) converter and variations of elements **2.10** to **2.15** and/or **2.24** to **2.33** of FIG. **2**. The I and Q signals provided by the **10***a*.5 splitter output are further spectrally shaped and limited by the set of I and Q channel LPF's, designated as Filt 2I and Filt 2Q. These optional (Opt.) F2I and F2Q Bit Rate Agile Filter(BRA) elements **10***a*.6 and **10***a*.7 in FIG. **10***a* are TCS and/or Long Response(LR) filters, where the term "Long Response" refers to the typically longer pulse and/or impulse response of the LR filters than that of the TCS filters. This cascaded TCS and conventional filter approach is applicable for bit rate agile spectrum enhanced GMSK signal generations, also designated as FGMSK containing elements related to U.S. Pat. No. 5,789,402 (for short '402); however, with the new single or multiple ACM Cross-Correlated (X) Single or Multiple Cos (C) and Sin (S) and/or Inverter (I) (for short "XCSI" and/or Peak Limiter (PL) processor components of this new invention.

The second optional (Opt.) filter set is **10***a*.6 and **10***a*.7. This set provides for processing of the I and Q signals provided by **10***a*.5. The XCSI unit **10***a*.8 cross-correlates the aforementioned I and Q signals with a C driven clock/sample/control and provides for selectable amount of cross-correlation between the I and Q channels, including for a cross-correlation reduced to zero, i.e. no cross-correlation between the TCS and LR processed signals. In some of alternate embodiments of this invention there is no cross-correlation apparatus used. In units **10***a*.9I and **10***a*.9Q optional additional filtering processing is implemented by optional units F3I and F3Q. These units provide optional ACM filtered/processed BRA cross-correlated or not-cross-correlated I and Q signals to the Quadrature Modulator unit **10***a*.10 which in turn provides the signal of amplification to Amplifier (Amp) **10***a*.11 and to output port **10***a*.12 for signal transmission or broadcasting. The output port is represented by connector **10***a*.12.

In FIG. **11***a*.1 a conventional Non-Return to Zero (NRZ) signal pattern is illustrated in **11***a*.1. In **11***a*.2 a modified Return to Zero (RZ) pattern designated as Feher Return to Zero (FRZ) data pattern is shown. Both of the NRZ and FRZ signals are Time Constrained Signals (TCS). The FRZ signal **11***a*.2 has an adjustable amount of Delay (D) for the forced transition instance from the logic state **1** to logic state **0**. The FRZ signal is used in some of the TCS embodiments, **11***a*.3 while in other TCS architectures FRZ is not in use. One of the advantages of FRZ signals is that they may contain discrete spectral lines and have a more robust performance in RF time dispersive or frequency selective faded systems if used in conjunction with modulators/demodulators, including but not limited to quadrature modems. The FRZ signal contains, in some embodiments, non-symmetrical or asymmetrical rise and fall times and even pulse shapes. The TCS unit **11***a*.3 has as its inputs one or more signals as well as the "C" signals where C designates optional clocks, and/or sampling including over- and/or under-sampling sig-

nals and/or other control signals. The TCS processor in one of the embodiments generates Non-Cross-Correlated (NCC) signals while in another embodiment Cross-Correlated (CC) signals are generated in unit **11***a*.3. In the case of digital processing such as FPGA and/or ROM and/or RAM, digital implementations D/A converter(s) **11***a*.4 are provided. In one of the embodiments a single D/A is implemented. The single D/A is providing time shared or time multiplexed signals as I and Q inputs for Quadrature Modulation (QM). Prior to QM an optional analog processor and/or filter with possible BRA clocked operation, **11***a*.5, is implemented. The QM **11***a*.6 provides BRA quadrature modulated signals to optional amplifier or cascaded amplifiers **11***a*.7 which could operate in a linear mode or partly linearized mode or in a fully saturated NLA power efficient mode. The aforementioned amplifier provides the signal to the Antenna **11***a*.8 or alternatively to the output port **11***a*.9 for signal transmission.

An alternate embodiment is shown in FIG. **11***b*. The implementation of a Bit Rate Agile (BRA) pre-processor with single or multiple wavelets (also designated as) Signal Element (SE) storage and/or inverter and of filtered SE and ACM processors is illustrated. On leads **11***b*.1 and **11***b*.2 respectively the Data Inputs (DI) and Clock (C) inputs are shown. Here the terms "Data Inputs" are synonymous with one or more digital or analog or hybrid combined digital/analog signals having 2 or more signaling states. The term "Clock" or for short "C" is synonymous with one or more clock signals, sampling and control signals as mentioned elsewhere in this disclosure. Pre-processor **11***b*.3 stores I and Q Signal Elements (SE) for BRA operation optionally controlled and/or clocked/sampled by the **11***b*.2 and **11***b*.4 signals/clocks. The pre-processor unit **11***b*.3 stores in one of the embodiments a large number of separate and distinct Signal Elements (SE), also designated as "wavelets", and provides the selected SE in appropriate order to the **11***b*.5 single or multiple D/A converter(s). The D/A converter (S) provides to unit(s) **11***b*.6 and/or **11***b*.7 I and Q signals for further BRA operation. Selectable filters designated as 1 to N and/or a bank of filters are used in one of the ACM embodiments of **11***b*.6 and **11***b*.7 and provide the I and Q signals to ports **11***b*.8 and **11***b*.9.

In FIG. **12**, including **12***a* and FIG. **12***b* predominantly analog components used in analog implementations and embodiments of this FQPSK and related transceiver embodiments are shown. In addition to some of the active components depicted in these figures, embodiments of the virtually same functions as those with analog components are implemented with passive analog components. The individual components are conventional off-the-shelf available components described in detail in prior art publications including patents and detailed descriptions of these components are superfluous. In particular in FIG. **12***a* analog implementation components for cross-correlated and non-cross-correlated BRA processed TCS and/or LR filtered and/or ACM signals are shown. In FIG. **12***a* unit **12***a*.1 is a "COS" that is cosine or sine wave generator. One of the well-known embodiments of **12***a*.1 is a readily available analog Free Running Oscillator (FRO). Unit **12***a*.2 is a "Direct Current" (DC) source while **12***a*.3 and **12***a*.4 represent an alternate COS source and a Square Wave Source, respectively. Even though COS and SIN sources are illustrated as separate components, embodiments include single source COS or SIN sources/generators which may be converted to Triangular Square Wave or other periodic or non-periodic sources. The aforementioned signal sources or signal generators are connected in a variety of configurations such as the exemplary embodiments of FIG. **12***a* and FIG. **12***b* to components such as multipliers, amplifiers, switches, attenuators, inverting amplifiers and "DC shift" units **12***a*.5 to **12***a*.12 for processing and providing signals for further processing including selective switching or combining.

In FIG. **12***b* another analog BaseBand (BB) embodiment using predominantly analog components is illustrated. Units **12***b*.1 to **12***b*.5 are signal sources such as previously described. Unit **12***b*.6 is a previously described clock/sample/controlled source abbreviated with the letter C. Unit **12***b*.7 provides selection and/or combinations and permutations of the signal sources with amplitude adjustments of the aforementioned signal sources which operate at the same rate in some embodiments and operate in asynchronous non-related bit rates to each other in other embodiments. Unit **12***b*.7 provides one or more signals to standard and readily available components such as **12***b*.8 to **12***b*.24. These components provide inputs to the "select" or "combine" unit **12***b*.25 which has at its input optional Control (CTL), Clock Bit Rate (CBR) and Control Sampling Time (CST) signals. One or more of these signals, by itself or in combination, may constitute multiple inputs and are synonymously further abbreviated and designated as "C" in several parts of this invention. Units **12***b*.26 and **12***b*.27 provide further signal processing for the outputs of **12***b*.25 and generate I and Q output signals.

In the embodiment of FIG. **13***a* an implementation comprising mixed analog and digital circuit components is shown. On lead **13***a*.1 the data input or DIN provides two **13***a*.2 signals for multiplexing control/logic processing and memory. In one of the embodiments, logic processing and memory storage/processing converts the input signal to a Trellis Coded (TC) baseband signal. Control signals present on leads **13***a*.3 serve as one of the inputs to the N by M (N×M) channel multiplexer and cross correlator and/or other TCS unit **13***a*.6. Analog inputs of **13***a*.6 could be generated by unit **13***a*.4 and further processed by analog components such as the set of components **13***a*.5 of this particular embodiment. Units **13***a*.7 and **13***a*.8 provide additional digital timing bit rate and sample clock scaling, n/m rate division and miscellaneous logic functions embodied by standard logic gates and/or DSP and/or Analog Signal Processing (ASP) components.

FIG. **14** shows an alternate design of the current invention including a bank of switchable filters/processors with Linearized Phase or Phase Linear (PL) and Not Linear Phase (NLP) Filters. Phase Linearization Components may be entirely deleted or, if included in this implementation, they may be switched in and out in this hybrid analog and digital transmit implementation of the transmitter. Unit **14**.1 is the embodiment of a TCS processor for time constrained signals with or without cross correlation implemented for FQPSK or FGMSK or FQAM or FMSK or related BRA signals. The output(s) of the **14**.1 TCS processor provides one or more signals to the optional D/A unit **14**.2. The outputs of the single or multiple D/A or of **14**.1, in case **14**.2 is not used, are provided to the cascaded I and Q filters and Switches **14**.3 to **14**.5. While the filters are indicated as LPF-1 to LPF-3, they have been implemented as low-pass, band-pass and high-pass filters providing the LR pulse response with or without phase equalization. These filters may be designed for Agile Cascaded Mis-Matched (ACM) systems. An alternate embodiment comprises TCS unit **14**.6 connected through optional D/A unit(s) **14**.7 to the bank of **14**.8, **14**.9 and **14**.10 selectable or combined switched phase equalized or non-phase equalized parallel and/or cascaded units LPF-1I, LPF-1Q to LPF-M1 and LPF-MQ filters. On output ports **14**.11 and **14**.12 the processed I and Q signals of the

aforementioned particular embodiment of this invention are available for further processing.

In FIG. **15** one of the predominantly digital BRA and ACM alternative implementations is shown. The embodiment of digital processor based implementation, followed by one or more D/A converters and BRA Long Response (LR) filters are shown in the architecture of FIG. **15**. The block diagram of FIG. **15** is an alternative embodiment of this invention having a TCS signal generator in cascade with the 2nd processor set of bandwidth spectral shaping LR filters. The LR filters are designated as LPF. The embodiments include analog and digital LR filters including combination and selections between LPF, BPF and HPF and other analog or digital filters. Data encoder **15.1** has at its input the "Input Signal" and the "C" signals. For simplification reasons of this and some other figures of this invention, the C signals are not always drawn on the respective figures and are not connected in the diagrams to all of the possible inputs. Following data encoding, implemented by conventional digital and/or analog components and/or DSP and/or software or firmware, the signals are provided to an encoding/logic processor which could contain a Shift Register (SR) unit **15.2**. A flag generator provides one of the output bits to waveform select logic **15.4** for processing. Address generators **15.6** and **15.9** provide addressing information to ROM units **15.5** and **15.6**. The ROM units are sampled and their content read out to DAC (Digital to Analog Converters) **15.7** and **15.14**. The outputs of the DAC units are provided to units **15.8** and **15.15** for further filtering and providing the output signals to ports **15.16** and **15.17**, the ports for the I and Q signals, respectively.

In one of the alternate Field Programmable Gate Array (FPGA) based implementations of the TCS processor of FQPSK and FGMSK readily available Xilinx Chip Model No. SC4005PC84-6 has been used. While in an other embodiment Xilinx SC400FPGA was used. Other implementations used Alterra and Intel devices. The wavelets used in one of the designs used 16 samples for 1 symbol time Ts duration while in an other embodiments used only 4 samples for 1 symbol time Ts. Each sample was encoded in one of the implementations into 10 bits/sample with D/A converters having 10 bit resolution, in other cases 4 bits/sample were used.

In one of the embodiments of FIG. **15**, a data encoder, 4-bit shift register, I and Q waveform select logic, address generators based on ROM implemented components, D/A converters, Clock and Sampling Generators and output latches are used. This particular design does not use a half-symbol physical delay component in one of the (I or Q) baseband channels. Rather, the half-symbol offset between the I and Q channel output waveforms is obtained by appropriate waveform selection procedure.

In FIG. **16** "Wavelets" or Basic Signaling Elements (SE), for FQPSK designated also as "Wavelets" and/or "Signal Components" or merely "Signals" are shown. This FIG. **16** depicts TCS Wavelets for enhanced performance FQPSK signal generation with a Cross-Correlation of A=0.7 and in particular for TCS wavelets with only four (4) signaling elements required for storage—suitable for high speed and integrated TCS and cascaded filter LR processing solutions. The appropriately assembled I and Q cross-correlated TCS sequence is provided to BRA Long Response (LR) filtering of I and Q channels. Signals **16.1**, **16.2**, **16.3** and **16.4** in FIG. **16**, also designated as S1, S2, S3 and S4, are illustrated across one symbol interval. For 4 signaling state systems one symbol corresponds to two bits, thus Ts=2Tb in duration. The S1 to S4 signals could be sampled and stored 4 times per symbol, i.e., 2 times per bit or at other sample intervals. The sampled signal wavelet values are stored in architectures containing memory devices. Signal element or "wavelet" S4, designated as **16.4**, is simply a DC component in this particular embodiment. In some of the TCS embodiments S1 to S4 are cross-correlated between the I and Q channels and have continuous derivatives at the signal transitions, while in other embodiments the TCS signals are not Cross-Correlated. Alternate embodiments have a more or lesser number of wavelets than illustrated in FIG. **16**.

An implementation of FQPSK baseband signal processor's taking advantage of inverse and symmetrical properties of its waveforms is described in this section related to previously described figures and embodiments and in particular in relation to FIG. **15**, FIG. **16** and FIG. **17**. Instead of the storing all the basic entire or whole "Wavelets" of the baseband signals, one of the implemented designs with ROM lookup table uses only 3 "basic" wavelets. To simplify the implementation of cross-correlated FQPSK baseband signals, we use the symmetry properties of the wavelets and the hold function for DC value. In the design there is a half-symbol delay between the I and Q channels so that the ROM contents in I and Q channels are the same. FQPSK and FGMSK eye diagrams at the TCS output and also at the cascaded TCS and LR filters are shown in FIG. **19**. As a specific design and teaching example the TCS generated eye diagram of an FQPSK signal an A=**0.707** cross-correlation parameter is shown in FIG. **19**(*c*). Such an eye diagram is measured and/or computer generated at the output of the embodiments shown in FIG. **10** or FIG. **11** and/or other disclosed embodiments, including at the outputs of the LR filters in BRA operation of the implementation of FIG. **15**, provided that the D/A converter has a good resolution accuracy e.g. 8 bits/sample and that the LR filter units **15.8** and **15.15** of FIG. **15** have a considerably higher cut-off frequency than the inverse of bit rate. It can be seen that in the FQPSK eye diagram of FIG. **19**(*c*) there are 10 kinds of waveforms or wavelets during half-symbol duration (from 0 to 8 or 0 to Ts/2). Thus it is possible to pre-calculate the waveforms directly from the input data. FIG. **15** shows one of the implementation architectures of the designed FQPSK baseband processor using this approach. In FIG. **16** the 3 half-basic waveforms needed to generate all the possible TCS response wavelets for FQPSK are shown. Based on the symmetry and inverse properties of the whole set of the wavelets illustrated in FIG. **19**(*c*), instead of 10 only 3 waveforms plus a DC value (holding function for DC value) are required. In this design, 4 samples/symbol (or 2 samples per bit) are used to implement the waveforms of FQPSK.

In FIG. **17**, BRA" Wavelets" for FGMSK are shown. These Gaussian wavelets are suitable for smaller size memory implementations, for bit rate agile GMSK signaling having a BTb=0.5 parameter. This FIG. **17** depicts TCS Wavelets for use in LR filtered enhanced performance reduced spectrum BRA systems. Only four (4) signaling elements are required in this embodiment of the TCS part of the FGMSK processor. With the embodiment of FIG. **15** and other alternate digital and/or analog embodiments these signals can be easily generated even at very high bit rates. The appropriately assembled I and Q cross-correlated TCS sequence is provided to BRA Long Response (LR) filtering of I and Q channels. In FIG. **17** the signals **17.1**, **17.2**, **17.3** and **17.4**, also designated as S1, S2, S3 and S4, are illustrated across one symbol interval. For 4 signaling state systems one symbol corresponds to two bits. Thus, Ts=2Tb in duration. The S1 to S4 signals could be sampled and stored 4 times per symbol, i.e., 2 times per bit or at other sample rates. The

sampled signal wavelet values are stored in architectures containing memory devices such as the previously disclosed ROM based embodiments. The FGMSK signal shapes have different shapes from the S1 . . . S4 signals illustrated in FIG. 16. In some of the embodiments for use in FGMSK the S1 to S4 wavelets are cross-correlated between the I and Q channels. In other embodiments for FMSK the signals are not cross-correlated, or have different cross-correlation algorithms and embodiments than in FGMSK and/or have continuous derivatives at the signal transitions. Alternate embodiments have a larger or smaller number of wavelets than illustrated in FIG. 16 and in FIG. 17.

In FIG. 18 Differential Encoding (DE) and Differential Decoding (DD) of FQPSK and FGMSK is shown. A difference between the DE of this bit rate agile FGMSK encoder from that of conventional GMSK is in the algorithm difference of these two DE and Corresponding Differential Decoding (DD) embodiments. The new DE for FGMSK is fully compatible and interoperable with conventional OQPSK; the DE of prior art bit rate agile GMSK is not.

Eye diagrams shown in FIG. 19 are hardware measured and computer generated diagrams for Cross-Correlated BRA signals at various measurement/display points. The eye diagrams of DE prototype BRA apparatus transmit signals are presented. In FIG. 19(*a*) FGMSK eye diagrams of I and Q baseband signals with BTb=0.3 are shown prior to the LR cascaded performance enhancement I and Q filters. In FIG. 19(*b*) eye diagrams of I and Q baseband signals of an FQPSK transmitter, operated in a BRA mode having a cross-correlation parameter A=0.7 after the BRA processor LR filters (I and Q filters) are shown. In this case the LR filters have a relatively high cut-off frequency relative to the symbol rate. In FIG. 19(*c*) an FQPSK computer generated eye diagram is illustrated. The I channel eye is shown, for a Xcor. Parameter A=0.7 prior to LR filters. The eye diagram contains only four (4) basic wavelets and represents a TCS eye pattern In FIG. 19(*d*) hardware measured FQPSK eye diagrams of I and Q signals are shown for a BRA operation displayed after the LR filters of the I and Q Channels. This particular FQPSK is designated as an FQPSK-B and it has a Xcor parameter A=0.7 followed by I and Q post TCS Low-Pass Filters having LR characteristics. In FIG. 19(*e*) the measured vector constellation of an FQPSK-B signal after the LR filters processors of an implemented prototype system is shown.

Description of Multi-state FQPSK, FQAM, FGMSK and FMSK

In this section of the detailed description of this invention the focus is on Quadrature Modulated (QM) multiple signaling state (for short "state") systems with more than 4 signaling states of the QM signal and more than 2 states in the respective I and Q baseband channels. In the previous section the focus was on the description of QM four (4) state FQPSK systems. These four-state systems have, in general, in the I and Q baseband channels 2 signaling states (for short "states") in the I channel and 2 states in the Q channel. Most implementations and embodiments of the 4-state systems apply to multi-state (more than 4-state) Quadrature Modulated systems, described in this Section, such as 9, 16, 49 or 64 or 256 state QM systems having 3, 4, 7, 8 and 16 states in their respective baseband channels. The technologies and embodiments described for the multiple state systems are also applicable for the implementations and embodiments of 4-state systems. Forward and Backward COMPATIBILITY and/or interoperability between the 4-state and, more than four-state, multiple state FQPSK and Feher's Quadrature Amplitude Modulation (FQAM) and multi-state FGMSK and FQPSK systems is a definitive advantage in new product developments. Additionally some of these systems are also backward compatible with the previously patented Feher BPSK (for short FBPSK and FMOD) systems, such as disclosed in [P1] and [P2] and the references in the aforementioned U.S. Patents and cited references.

A multi-state QM architecture for 4 or more than 4 states, designated as FQAM is illustrated in the embodiment of FIG. 20. In this implementation block diagram of an FQAM multi-state Cross-Correlated BRA Transmitter a single RF Amplifier operated in fully saturated NLA mode or Linearized (Lin) mode of operation is used. The Input Signal is connected to an optional Encoder unit 20.1. This unit, if used includes logic processing and Encoding functions such as Trellis Coding or CRC or FEC or DE or Gray Coding, Serial to Parallel conversion and/or other digital processing functions. In one of the embodiments an optional S/P (Serial to Parallel) converter, unit 20.2 is included to process the signals received from 20.1. The Signal Mapper 20.3 maps the binary signals from 2 states to M states (levels) and includes in some of the embodiments Cross-Correlation between the binary and/or between the converted multi-state signals. The outputs of the Signal Mapper TCS unit 20.3 are connected to D/A converters 20.4 and 20.5. The D/A Cross-Correlated BRA signals are TCS multilevel Cross-Correlated signals with variable and/or presetteable Xcor. In alternate embodiments no cross-correlation between the I and Q signals is implemented. The D/A outputs are fed to 20.6 and 20.7 filters, indicated in the drawing as LPF. These filters are LR filters and are implemented with IIR digital or IIR analog filters or a combination of conventional analog or digital filters. The BRA signals, which have been Cross-Correlated and are TCS in cascade with LR signals are provide to the inputs of Quadrature Modulator(QM) 20.8. The QM has an unmodulated Carrier Wave input from unit 20.9. The Quadrature Modulated signal is processed by an optional "Roofing Filter" to remove higher order spurious components and is fed to amplifier 20.12 and to antenna 20.13 or output port 20.14. An optional Pilot Tone or Multiple Pilots are added to the RF signal by Pilot Generator/adder 20.11. Combining adding of pilot signals is achieved by hardware combiners or by adding Unmodulated signals over the air through a separate antenna.

A 16 state FQAM embodiment is illustrated in the implementation architecture and block diagram of FIG. 21. This architecture can be extended and/or modified to 64 state or to other larger or smaller number of signaling states. In simple terms NLA Quadrature Modulated systems are generated by FQPSK or FGMSK or FMSK type of 4 state QM embodiments (for short the generic term "FQPSK" is also used) as described in earlier sections of this invention. If two NLA four state RF signals are combined than a 16 state NLA signal is obtained. If three NLA four state RF signals are combined than 64 state NLA signal is obtained. If four NLA four state RF signals are combined than a 256 state NLA signal is obtained and the number of signal states can be further increased by the aforementioned extension of the multiple signal combining process. The term "combining" or "Combiner" or RF signal addition in FIG. 21 is accomplished by an RF hardware combiner. Off the shelf, readily available components, such as Hybrid Microwave Combiners, are suitable for hardware RF combining. On lead 21.1 in FIG. 21 an input NRZ data signal is provided to the input ports of the Serial/Parallel(S/P) Converter 21.2. Four parallel data signals, designated as I1, Q1 and I2, Q2 are provided to FQPSK (or FGMSK or FMSK) modulators 21.3 and 21.4. One of the embodiments and/or implemen-

tations of FQPSK previously disclosed in the detailed description of this invention implements 21.3 and 21.4. The FQPSK signals are provided to Optional (Opt) preamplifiers, which operate in Linearized(LIN) or NLA mode. The High Power Amplifiers (HPA) 21.7 and 21.8 provide the RF amplified modulated signals to RF Combiner 21.9, which in turn provides the NLA combined 16-state signal to the output port 21.10.

In Seo/Feher [9] and [P4] and [6; 8] prior art references, implementation architectures of NLA systems operated in 16-QAM, 64-QAM, 9-QPRS, 81-QPRS and other quadrature modulated systems have been described and/or referenced. The aforementioned prior art does not include NLA cross-correlated, filtered and bit rate agile NLA systems for QAM disclosed in this invention, and in particular related to the discussion of FIG. 21 and FIG. 22. Based on these Feher et al. references, one of the embodiments, is related to the architectures of FIG. 21. To obtain a 16-state QAM with cross-correlated FQPSK signals that are NLA through HPA1 and HPA2, the RF amplifiers and RF combiner are adjusted to have an RF combined output fed to RF combiner, unit 21.9, which provides the RF combined output 21.10. The RF combined output power generated by unit 21.7—HPA1 is 6 dB higher than the RF power provided to output 21.10 by HPA2 designated as unit 21.8.

FIG. 22 is the implementation architecture of "Over the Air Combined" FQAM signal generation by implementing 2 or more FQPSK and/or FGMSK type of signals. In FIG. 22 instead of the use of a hardware embodied RF Combiner to combine the HPA1 and HPA2 signals, the output signals of HPA1 and HPA2 are fed to two separate antennas and transmitted as wireless signals "over the air." In this architecture RF Combining is achieved "Over the Air" that is the RF signals are transmitted over a wireless medium and combined in the receiver antenna.

The baseband processor, quadrature modulator and signal amplifiers architecture of the NLA signals, "Over-the-Air Combined," is closely related to that of FIG. 21 which uses the hardware RF combiner. The input NRZ data on lead 22.1 is provided to a Serial/Parallel (S/P) unit 22.2 which provides 4 parallel signals two FQPSK quadrature modulators, units 22.3 and 22.4. The quadrature modulated signals are provided to amplifiers, and in particular, to optional NLA 22.5 and to High Power Amplifier (HPA) 22.7 in the upper part of the figure. HPA-1, unit 22.7 provides the RF modulated signal to antenna 22.9 or to an output port 22.11. In the lower branch the FQPSK modulator, unit 22.4, provides the quadrature modulated signal to optional NLA 22.6 and to HPA-2, unit 22.8. The amplified signal of 22.8 is provided to antenna 22.10 and/or to output port 22.12.

To obtain a 16-state QAM with cross-correlated FQPSK signals that are NLA through HPA-1 and HPA-2, the RF amplifiers and RF combiner are adjusted to have an RF combined output fed to antenna 22.9 and/or output port 22.11, 6 dB higher in power than the RF power provided to antenna 22.10 and/or output port 22.12.

FIG. 23 shows the embodiment of an Orthogonal Frequency Division Multiplex (OFDM) type of embodiment with FDM signal combining of a number of FQPSK type of Lin or NLA signals. In one of the embodiments of this invention RF Combining is implemented by hardware RF components while in an alternative implementation the RF combining is implemented with "Over the Air Combined" signals. If multiple antennas are used, then this architecture is also known as an "Antenna Array" (AA) architecture. Lead 23.1 containing the Input Data (ID) is provided to a Serial-to-Parallel (S/P) converter, unit 23.2, having M set of outputs where one output set constitutes a separate I and Q signal or a serial data stream. The S/P converter 23.2 may contain an optional cross correlator (Xcor). As the input signal is S/P converted, the data rates on the 1, 2, . . . , M input leads to the bank of FQPSK modulators 23.3 are at an M times reduced data rate compared to the input data rate. As an illustrative example of this architecture, if the input data rate is Fb=10 Mb/s and there are 100 FQPSK modulators (M=100), then the bit rate of individual FQPSK modulators is 10 Mb/s: 100=100 kb/s. The aggregate transmission rate of such a system is not changed. The aforementioned parallel data are provided to M modulators designated as FQPSK.1, FQPSK.2, . . . , FQPSK.M, collectively referred to as unit 23.3. These modulated signals are provided to a set of RF amplifiers, 23.4 and optional RF Switches units designated as 23.6. The M amplified signals are provided in one of the embodiments through RF combiner 23.7 to a single antenna "Ant.C" unit 23.8 or port 23.9. In an alternate use the M modulated and amplified signals at the outputs of RF amplifiers 23.4 are provided to the antenna array 23.5 designated as Ant.1, Ant.2 . . . to Ant.M. If the Antenna Array architecture is used, then the M signals are "Over the Air Combined" signals. If a hardware RF combiner 23.7 is used with a single antenna 23.8 or output port, then the architecture represents a hardware combined embodiment. An advantage of the "Over the Air Combined" architecture is that all RF amplifiers within the set 23.4 may operate in fully saturated NLA power efficient mode.

FIG. 24 is an alternate Antenna Array and RF Combining implementation architecture of multiple FQPSK type of signals. This figure illustrates multiple TCS and/or filtered BB processors connected to an antenna array and/or RF combiner. Input lead 24.1 contains an input signal or a multitude of signals, which could comprise analog signals, digital binary or digital multilevel signals, or other signals, for short "Input Signal." Unit 24.2 receives the input signal and processes it with a TCS containing optional LR filters and/or a 1^{st} set of cross correlators (Xcor) for FQPSK signals. A Bit Rate Agile clocked bank of filters 24.3 receives the signals of 24.2, processes them and provides to unit 24.4 which is an optional 2^{nd} set of Xcor and/or TCS with LR response filters and/or Peak Limiter (PL) devices. The signals from 24.4 are provided to Quadrature Modulators 24.5 and to a bank of amplifiers 24.6 in the figure illustrated as FA1 to FA3. The RF amplified signals are provided to antenna array 24.8 or to RF combiner 24.9 through the set of RF switches 24.7. The RF combined output is provided to antenna 24.10 or alternately output port 24.11.

In FIG. 25 an alternate implementation of encoding and signal mapping of FQPSK, FQAM and FGMSK signals is shown. In the embodiment of FIG. 25 a trellis coded implementation with an appropriate signal mapping for trellis coded generic FQPSK without the need for redundancy is shown. In addition to trellis coding other coding algorithms are suitable for the shown implementation architecture. The aforementioned other encoders include non-redundant Differential Encoding (DE), Gray encoding, encoding/conversion of NRZ signals into RZ or FRZ signals or Manchester or other sets of signals. Encoding for error correction and detection may require the insertion of redundant bits and Forward Error Correction (FEC) encoders such as Block Encoders including Reed-Solomon, BCH, convolutional, CRC and other encoders are among the illustrative embodiments of encoders suitable for FIG. 25. The specific trellis encoder schematic diagram and signal mapping part of FIG. 25 is based on Simon/Yan's published

reference [22], which includes logic/encoding 25.3 and signal mapping 25.4. The aforementioned reference does not disclose embodiments for TCS and LR filtered changeable amount of cross correlated and of filtered Bit Rate Agile (BRA) and/or Peak Limited (PL) implementations and of Agile Cascaded Mis-Matched (ACM) filtered systems having single or multiple I and Q readout tables with compressed memory elements.

In FIG. 25 trellis coded TCS and LR filtered FQPSK signals having BRA applications with or without Cross-Correlation and with and without Peak Limiting (PL) circuits in the I and Q channels are shown. The digital processing parts of the trellis or other encoder precede the additional TCS and LR and other processors in the implementation embodiment of FIG. 25. In alternate embodiments the digital encoder with and without trellis coding is integrated in one block and one function with parts or all of the TCS and LR blocks or the order of processing is changed.

Illustrative Performance of Exemplary System

The performance of illustrative and some of the "best-illustrative" embodied FQPSK and related BRA systems of this invention is highlighted. This invention includes numerous embodiments and has a large class of subsystems and implementation details as well as designations. For this reason the term "best-illustrative" is used herein. For some users and designers "best" means the narrowest possible spectrum at a Power Spectral Density (PSD) of about −20 dB to meet certain FCC mandated requirements, while for other users the "best" PSD is defined at −70 dB for others "best" refers to best Bit Error Rate (BER) performance in an Additive Wide Gaussian Noise (AWGN) operated environment, while for some others the "best" or "optimum" BER=f(Eb/No) performance is most desired. Other categories of the term "best" could mean fastest synchronization or re-synchronization of a receiver/demodulator or "best" BER performance or smallest number of outages in an RF delay spread-frequency selective faded environment with the "best," that is, fastest and highest performance adaptively equalized demodulators. A large category of designers and users of this invention might define "best" as the lowest cost commercially available equipment from numerous sources having the highest spectral efficiency simultaneously with the smallest size for a certain RF power and the "best," i.e., maximal Bit Rate Agile (BRA) flexibility and/or interoperability and compatibility with previous generations and implementations of FQPSK and/or of other "legacy" systems. For the aforementioned reasons the term "best illustrative" is used in the performance attained with some of the aforementioned "best" implementations.

As an illustration of one of the "best illustrative" NLA spectra, the Power Spectral Density (PSD) of NLA wireless/telemetry system is illustrated in FIG. 26. The multiple data links in these telemetry systems are operated at specific bit rates of 13 Mb/s rate per link. The spectra shown in FIG. 26 are typical for spectral usage in the U.S. for the U.S. Government-authorized band of 2200 MHz to 2290 MHz for Government applications. In FIG. 26 one or more of the modulated and received signals is shown to be in the 18 dB to 20 dB lower than that of adjacent signals. In "real-life" systems it is often the case that the desired signal power is about 20 dB lower in power than that of the adjacent signals. With telemetry standardized filtered PCM/FM systems, at the aforementioned 13 Mb/s rate, 3 data links can be used simultaneously. During the 1990s, filtered PCM/FM systems have been extensively used. With emerging FQPSK systems and in particular Draft Standardized FQPSK-B systems the number 13 Mb/s rate links is doubled to 6, while with 16-state FQAM, also designated as FQPSK.2.4 the number of 13 Mb/s links is quadrupled (over that of standardized PCM/FM) to 12 data links. Thus the spectral efficiency of FQPSK is double that of standardized filtered PCM/FM and the spectral efficiency of FQAM with 16 states and operated also in an NLA mode is quadruple that of the standardized filtered PCM/FM systems.

From FIG. 26 illustrated spectra it is noted that the Integrated Power from the adjacent channels falling into the desired channel may have a significant impact on the performance of the desired channel. In the referenced publications and patents the importance of Integrated Adjacent Channel Interference (ACI) is highlighted and described. For this reason the Power Spectral Density (PSD) and the ACI of Linearly (Lin) and of NLA transmitted FQPSK and GMSK signals is shown in FIG. 27. The PSD and Integrated ACI of hardware measured prototype FQPSK-B in a NLA transmitter and of a BRA linearized (Lin) transmit FQPSK is illustrated in the upper part of FIG. 27. In the lower part of FIG. 27 the Integrated Adjacent Channel Interference of FQPSK systems with that of GMSK systems is compared. In this figure "W" denotes the frequency spacing between Adjacent Channels. In case of GMSK which has been implemented with BRA embodiment described in this invention and designated as FGMSK having a Gaussian filter and bit duration (Tb) product of 0.25 has been used in the computed ACI result shown in FIG. 27. The computed ACI of a BTb=0.25 filtered system with considerably steeper filters than that of conventional Gaussian receive filters was simulated by JPL/NASA. The ACI curves for FQPSK-B and FQPSK-D1 as well as FQPSK-Lin are also included. Note from the results the significant(approximately 2 to 1 at −60 dB) spectral ACI advantages of FQPSK over that of GMSK systems.

Multi-state FQAM systems such as 16-state FQAM designated also as FQAM-16 and FQPSK.2.4 (the first number in this latter abbreviation indicates 2^{nd} generation FQPSK while the 2nd having 4 signaling states per I and per Q channel). In NLA systems have approximately double the spectral efficiency of the already-spectrally-efficient FQPSK systems including BRA systems operated in an FQPSK-B mode disclosed in this invention. The abbreviation "FQPSK-B" is a designation for cross-correlated FQPSK systems having an embodiment in which the TCS cross correlators are cascaded with LR filters operated in a BRA mode. The substantial spectral saving attained by 16-state FQPSK systems over alternative conventional 16-QAM pre-RF amplification filtered systems is illustrated by the computer-generated results shown in FIG. 28.

In FIG. 28 the ACI results of illustrative FQPSK.2.4 (also designated as FQAM-16) state systems, obtained after fully saturated NLA, are compared with that of NLA conventional pre-modulation filtered 16-state QAM systems. The spectral efficiency advantage of the illustrated FQAM is more than 200% over that of prior art QAM at −30 dB and FQAM has an even more significant spectrum advantage in terms of ACI at the critical −40 dB to −60 dB range. High performance systems require a robust BER performance in Additive White Gaussian Noise (AWGN) and also other interfering and noise environments. A frequently-used performance indication is the BER performance as a function of the available Energy of a Bit (Eb) to Noise Density (No) ratio. For RF power efficient as well as spectrally efficient systems having a robust BER, the NLA system performance in terms of BER =f(Eb/No) is specified for numerous system applications. In particular, in FIG. 29 the performance of FQPSK is highlighted.

FIG. 29 The BER performance, in terms of BER=f(Eb/No), of prototype measurements and Computer design/software generated data of FQPSK systems illustrated that NLA FQPSK is within about 0.5 dB of the ideal theoretical LIN amplified QPSK systems. Simple bit by bit detection as well as trellis decoding without redundancy has been used. In FIG. 29 curve (a) represents an ideal theoretical linearly (LIN) amplified system, while curve (b) represents a BER optimized NLA-FQPSK, and curve (c) represents a BRA and MM hardware-prototype measured FQPSK-B system performance, prior to optimization.

Detailed Description of Exemplary Embodiments of Receivers and of Demodulators

Receivers and Demodulators are described in this section. Signal reception, adaptive equalization, demodulation, fast and robust synchronization, bit recovery, Non Redundant Error Detection (NED), online in service monitoring, Non Redundant Error Control (NEC) and new architectures and embodiments for Bit Rate Agile (BRA) and NLA cross-correlated FQPSK, FQAM and related systems are disclosed in this part of the invention.

In FIG. 30 a generic receiver and demodulator is shown. In this FIG. 30 demodulation of FQPSK type of signals, by using quadrature demodulation structures such as QPSK, QAM and OQPSK demodulation, enhanced by the architectures of the embodiment, illustrated in this figure is accomplished. Fast signal acquisition is attained and numerous other performance enhancements are achieved by the disclosed generic embodiment of this demodulator. Input port and lead 30.1 obtains a modulated signal from a receive input port. The optional BPF unit 30.2 is provided in some of the embodiments in which excessive strength out-of-band/or adjacent channel signals degrade the performance of the subsequent circuits if this "protection" or "roofing" BPF is not present. Automatic Gain Control (AGC) circuit 30.3 operates in a linear or in a non-linear (NL) mode. For some applications an advantage of FQPSK and FQAM type of signals is that they are suitable for nonlinear AGC operation. From the prior art it is well known that nonlinearly operated AGC circuits such as "hard-limiters" and "soft-limiters" have faster AGC operation than their linear counterparts and in certain environments nonlinear AGCs outperform linear AGCs and in particular regarding "weak signal suppression" and also lead to reduction of Co-Channel Interference and of Inter-Symbol Interference (ISI) caused by certain RF delay spread—frequency selective faded environments. The optional AGC provides the quadrature demodulator 30.7 and follow-up signal processors including LPFs 30, Analog/Digital (A/D) 30.10, Symbol Timing Recovery (STR) 30.6, Adaptive Equalizer (AE) which could be a blind equalizer 30.11 and digital logic circuits decoders 30.12 to 30.17 the signals for demodulation and decoding. Additional signal processors which enhance the performance of the receiver/demodulator of this invention include one of the following: switchable changeable Carrier and Symbol Recovery unit 30.18, Pilot Extraction for unambiguous carrier recovery, fast AGC, and Automatic Frequency Control 30.19. Non-Redundant Error Detection (NRED) unit 30.20, Diversity Switching Combining Controller 30.21 and Pseudo-Error On-Line Monitor 30.22 units are also included.

FIG. 31 is a demodulator architecture also known as a "Block Demodulator" and/or digital demodulator or software demodulator. This implementation/embodiment is used for software or firmware or hardware, or combined hybrid implementations of this invention. On receive port/lead 31.1 the received RF signal or the received RF signal down-converted to a convenient IF frequency or to the baseband frequency range is shown. Unit 31.2 is an optional "roofing" BPF or other filter to protect the front end of the A/D 30.3 unit from out-of-band signal overload. The A/D provides serial or parallel signals for further digital processing, decision making and decoding in unit 31.4. The data is provided to output port 31.5.

FIG. 32 shows Antenna Arrays (AA) in this multiple transmit and receive with omni and/or directional antenna embodiment. This architecture with Adaptive Antenna Arrays (AAA) has the potential to increases the NLA spectral efficiency of FQPSK, FQAM and FGMSK systems to more than 30 b/s/Hz by processing the transmit and/or receive antenna signals in a directional mode. An interesting prior art reference is Winters [23], which contains several system applications of system applications of conventional non-patented modulated systems. The potential advantage of the embodiment of FIG. 32 for FQAM and FGMSK systems as due to the fact that the FQPSK and FQAM type of systems are suitable for NLA power and RF spectral efficient robust performance operation with single, dual and multiple antennas. Larger number of AA further increases the spectral efficiency and thus capacity of the systems of this invention in specific geographic areas covered by the AAs and AAAs.

FIG. 33 shows a Pseudo-Error (PE) on-line, or in-service monitor generic block diagram with on-line Probability of Error (Pe) monitor, diversity control, adaptive equalization control and Non-Redundant Error Control circuit also designated as Feher's Non-Redundant Error Control (FN) detection and correction. Non-intrusive on-line, also known as in-service bit error or Bit Error Rate (BER) or Probability of Error (Pe) monitoring of received signals has numerous benefits for the user of digital communication systems. Prior art references including Feher's [1,2,3] and the references contained therein describe the operational principles and some of the embodiments of the so-called "Pseudo-Error" on-line bit error detectors." While pseudo-error detection by itself is known from the prior art, pseudo-error monitoring of cross-correlated and filtered BRA systems combined with pseudo-error monitor generated control signal generation for adaptive equalization and/or diversity control techniques and embodiments are part of this new invention.

Pseudo-Error (PE) operation, adaptive equalization and diversity control signal generation by PE generated signals is described in relation to FIG. 33. On lead 33.1 the received RF signal is present. This signal could be converted to a convenient IF and/or near the baseband frequency range and could be RF selective faded and/or corrupted by interference. In FIG. 33 an FQPSK received modulated signal is illustrated; other types of modulated signals could be also processed with the PE based structures of FIG. 33. In addition to signal distortion, exhibited in terms of ISI, caused by RF selective, time-dispersive propagation channels Interference 33.2 and Additive White Gaussian Noise (AWGN) 33.3 is assumed to be corrupting this system by having interference and AWGN added to the desired signal path in 33.4. Following the selective faded signal path and interference and noise, the power splitter 33.5 provides the signal to I Channel Demodulator 33.7, 33.8 and 33.9 and Q channel demodulator and to the Carrier Recovery(CR) unit 33.6. The regular demodulated and regenerated data is present as "Data out to parallel to serial converter" in the I and Q channels. The PE circuit or "Pseudo-error on-line detector" has at its input stage an input port, designated as a buffer amplifier 33.10, followed by the 33.11 LPF(Low-Pass Filter in the "pseudo" path (lower case "p" in the abbreviation) and the regenerator or threshold detector 33.12. Unit 33.13 is a clocked Exclusive-OR (ExOR) circuit

which has the regular demodulated "Data out to parallel to serial converter" as one of its data inputs "In1" and has the regenerated data from the pseudo data regenerator **33.12** as its 2nd data input "In2". The clocked ExOR circuit (the clock input is not drawn to the ExOR-to simplify the drawing) **33.13** provides binary pulses to the Pp(e) to P(e) converter **33.14**. Unit **33.14** is implemented by simple logic and counter circuits and/or as part of a micro-processor and by software, hardware or firmware.

Pseudo-Error(PE) implementations and their operating principles have been described in the literature, including references [1,2,3]. Unit **33.14** provides a signal to the Non Redundant Error Control (NREC) circuit **33.19**, which is used, for display of the actual estimated Pe or BER of the data stream. Implementations of PE detectors, described in the aforementioned references, or variations of PE detector implementations used in this invention serve as Adaptive Equalizer(AE) control signal generators and Control Generators for Diversity Combining and/or fast synchronization systems. In one of the structures of this invention **33.14** provides one or more signal lines to the Adaptive Equalizer Controller **33.17** and in turn to the Adaptive Equalizer (AE) **33.18**. The AE provides to output ports **33.20** and **33.21** control signals.

In FIG. **34** an implementation block diagram of a Pseudo-Error (PE) controlled IF adaptive equalizer of this invention, designated as Feher Equalizer ("FE") is shown. The elements, described in conjunction with FIG. **33**, described previously are used in this structure of FIG. **34**. At the input lead **34.1** the received RF or IF signal is provided to splitter **34.2**. The splitter output, designated as *i*(t) is fed to a signal combiner **34.4***b*. The lower branch of the splitter provides an input to signal multiplier **34.3**, followed by delay element D1 and the multiplied and delayed signal is fed to the second input of combiner **34.4***b*. The combiner output is fed to an IF to baseband quadrature demodulator unit **34.5**. The multiplier unit **34.3** receives at its second input one or more control signal (s), designated as c1(t) and generated by the PE monitor loop. The aforementioned multiplier **34.3** serves as a controlled signal attenuator, that is, it provides a time variable attenuation(or time variable gain) in the lower branch of the "one tap" adaptive IF equalizer comprising splitter **34.2**, combiner **34.4***b*, multiplier (also designated as mixer) **34.3**, delay element D1 **34.4***a* and combiner unit **34.4***b*.

The Demodulator **34.5** of FIG. **34** has a structure such as the I and Q channel demodulators shown in FIG. **33**. The demodulated "eye" diagram (for definitions and terms such as eye diagram-see one of the references listed, including [1, 2 or 3]) through interface **34.6** provides the data output via threshold regenerator and logic **34.7** to output port **34.8** and the clock to **34.9**, while the signals to the PE monitor are on leads **34.10** and **34.11**. Single or multiple lead signals on lead(s) **34.13** are provided to LPF **34.12** for signal shaping and/or processing and for providing the aforementioned c1(t) control signal to one of the inputs of the multiplier **34.3** of the adaptive equalization system. The operation of the adaptive Feher Equalizer (FE) shown in FIG. **34** operates in a baseband to IF feedback loop in which the control signal is generated by a PE detector. The PE signal is a binary fully regenerated signal thus it is not the same type of signal as used to control the coefficients of conventional adaptive taps of adaptive equalizers.

FIG. **35** is a diagram of a multiple delay switchable Adaptive Equalizer (AE) designated as Feher Rake "FR". A Non-Redundant Error Control (NEC) detector, such as a Pseudo-Error (PE) circuit based NEC is used to generate one or multiple control signals, designated as "Control Select Signals". Received signal on lead **35.1** is provided to multiple splitter ports **35.2**, **35.6** and **35.10**. The splitters provide signals to variable gain amplifiers A1 to An to provide signals to delay components D1 to Dn. The respective components are: **35.2** to **35.14**. The upper and lower branches of the split signals are re-combined in adders **35.3**, **35.7** and **35.11**. The signal selection switch, Switch unit **35.14** selects one of the IF signals present at **35.3**, **35.7** and **35.11** combiner outputs. The signal selection is controlled by the "Control Select Signals" generated by unit **35.21**. The selected signal at the output port of switch **35.14** is provided to **35.15** demodulator and PE monitor NEC detector. Output port **35.16** provides signals to **35.19** Pseudo Error NEC detector additional processing and in turn for signal shaping by a LPF **35.20** for providing signals to the Control Select Generator **35.21**. The FR is a combination of an adaptive Feher Equalizer (FE) with selectable and switchable delay components among several branches or "rake branches" of the receiver structure. In this embodiment the receiver operates based on the principle that if the PE detector and/or alternate NEC circuit has a relatively high Pe on line state then one or more of the component values of the delay elements will be switched out or in, that is selected, and similarly the gain values of the adaptive equalizer A1, A2, . . . , An will be changed, continuously or in discrete steps.

In FIG. **36** an implementation architecture for multiple Adaptive Feher Equalizers (FE) and Feher Rakes (FR) with one or more demodulators is illustrated. The received signal on lead **36.1** is provided to splitter port **36.2** and the splitter provides signals to units **36.3**, **36.4** and **36.5**. These units are FE and FR based on the previously described embodiments. These units provide signals to units **36.6**, **36.7** and **36.8** for multiple signal demodulation. Single or multiple PE monitor (s) **36.10** provide control signals to select by selection switch **36.9** the best signal.

FIG. **37** shows a 2-branch diversity receiver with an adaptive equalizer and a single demodulator. In this embodiment FQPSK and/or FQPSK type of signals are first combined, in combiner unit **37.6** and are afterwards Adaptively Equalized in unit **37.7**. Receiver antennas **37.1** and **37.2** provide signals to RF mixers/down-converters **37.3** and **37.5**. Oscillator and/or Frequency Synthesizer **37.4** provides Carrier Wave signals for down-conversion. The IF down-converted signals are provided to combiner and/or switch unit **37.6**, followed by adaptive equalizer **37.7**, by optional Linear or NLA amplifier **37.8** and by Demodulator **37.9**. The output demodulated data is available on port **37.10**, the received/bit synchronized clock on port **37.11** and additional timing, such as symbol timing or block sequence timing on **37.12**. One or more of the units and elements of this invention, described in conjunction with previous figures are used in the architecture of this FIG. **37**. The PE and/or other NEC generated control signals provide for best possible combining, including "Equal Gain Combining", "Weighted Gain Combining", "Selective Combining" and other combining methods described in the prior art literature.

A fundamental difference is that in this invention the actual Pseudo-Error rate is used as the pre dominant control signal generator and the PE monitor selects and/or combines the best performance BER signals, while the prior art combiners select or combine based on the received Carrier Power or received Carrier-to-Noise (C/N) ratio. Combining or selecting signals, based on received C/N or received carrier power (C) may lead to the selection of the inferior performance channel or combing with the wrong ratio or wrong weight, and in particular if the RF channel has serious frequency selective fades.

For example the "main RF signal" designated RF main from antenna 37.1 has in one instant a much higher received carrier power than the carrier power on RF diversity antenna 37.2. Based on prior art receivers, combiners and diversity selection criteria the "main" signal would be selected as it has a higher C and thus higher C/N. However, in a severe RF selective faded environment even though the C power of the main branch, antenna 37.1 is much larger than that of the diversity antenna 37.2. In this instance the main antenna signal has much more RF frequency selective fade thus much worse performance the prior art receiver would choose/select the main branch with its poor and inferior performance, while the PE and/or other NEC based control signal disclosed in this invention would select the diversity signal with its superior performance.

Additional Description

Having now described numerous embodiments of the inventive structure and method in connection with particular figures or groups of figures, and having set forth some of the advantages provided by the inventive structure and method, we now highlight some specific embodiments having particular combinations of features. It should be noted that the embodiments described heretofore, as well as those highlighted below include optional elements or features that are not essential to the operation of the invention.

A first embodiment (1) provides a bit rate agile communication system comprises a splitter receiving an input signal and splitting the input signal into a plurality of baseband signal streams; a baseband signal processing network receiving the plurality of baseband signal streams and generating cross-correlated cascaded processed and filtered bit rate agile (BRA) in-phase and quadrature-phase baseband signals; and a quadrature modulator receiving and quadrature modulating the cross-correlated filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated output signal.

A second embodiment (2) further requires of the bit rate agile communication system that the baseband signal processing network includes a cross-correlator and at least one bit rate agile cascaded mis-matched (ACM) modulator filter.

A third embodiment (3) further requires of the bit rate agile communication system that it comprise: a demodulator structure having at least one bit rate agile (BRA) cascaded mis-matched (ACM) demodulation filter which is mismatched (MM) to the cascaded processed and filtered modulated signal, and operating to demodulate the bit rate agile signal.

A fourth embodiment (4) further requires of the bit rate agile communication system that the at least one processed and filtered baseband signal is generated by a plurality of modulator filters, and at least one bit rate agile (BRA) demodulator filter is used for signal demodulation.

A fifth embodiment (5) further requires of the bit rate agile communication system that the plurality of modulator filters, and the demodulator filter are connected in either serial, parallel, or a combination of serial and parallel topology.

A sixth embodiment (6) provides bit rate agile communication system comprising: a baseband signal processing network receiving parallel baseband signal streams and generating combined Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals; and a quadrature modulator receiving and quadrature modulating the Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated bit rate agile output signal.

A seventh embodiment (7) further requires that the bit rate agile system further comprise: a transmit amplifier receiving the quadrature modulated output signal and generating an amplified transmit signal for coupling to a transmission medium.

An eighth embodiment (8) further requires that the bit rate agile system further comprising a demodulator receiving and demodulating the bit rate agile transmit signal.

A ninth embodiment (9) provides in a communication system, a method for generating bit rate agile signals comprising steps of: receiving an input signal and converting the input signal into a plurality of signal streams; processing the plurality of signal streams to generate cross-correlated signals having changeable amounts of filtering for bit rate agile in-phase and quadrature-phase baseband signals; and modulating the cross-correlated filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated bit rate agile output signal.

A tenth embodiment (10) provides in a signal transmission system, a method for generating bit rate agile signals comprising steps of: receiving a plurality of signal streams; processing the plurality of signal streams to generate cascaded Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals; and modulating the Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals to generate a quadrature modulated bit rate agile output signal.

An eleventh embodiment (11) provides a Bit Rate Agile (BRA) structure comprising a input port for receiving input data; a splitter having an input coupled to the input port, and serving to split the input data into baseband signal streams; a baseband signal processing network for receiving the baseband signal streams and providing cross-correlated and filtered Bit Rate Agile (BRA) in phase and quadrature phase baseband signals; a Quadrature Modulator serving to quadrature modulate the cross-correlated filtered in phase and quadrature phase baseband signals; an interface transmitter port to provide the quadrature modulated signal to the transmission medium; an interface receiver port to provide connection of the the cross-correlated filtered quadrature modulated signal to the demodulator; and a demodulator structure to serve for Bit Rate Agile (BRA) signal demodulation having Bit Rate Agile (BRA) demodulation filters Mis-Matched (MM) to that of the modulator filters.

A twelth embodiment (12) further requires of the Bit Rate Agile (BRA) structure structure that the processed in phase and quadrature phase baseband signals have amplitudes such that their vector sum is substantially constant and has reduced resultant quadrature modulated envelope fluctuations.

A thirteenth embodiment (13) further requires that the Bit Rate Agile (BRA) structure comprises means for selectively reducing the cross correlating factor down to zero.

A fourteenth embodiment (14) provides a Bit Rate Agile (BRA) structure comprising a baseband signal processing circuit receiving one or more baseband signal streams and providing cross-correlated and filtered Bit Rate Agile (BRA) in-phase and quadrature-phase baseband signals; a quadrature modulator serving to quadrature modulate the cross-correlated filtered in phase and quadrature phase baseband signals; a transmit amplifier to provide the quadrature modulated signal to the transmission medium; an interface receiver port to provide connection of the the cross-correlated filtered quadrature modulated signal to the demodulator; and a demodulator structure to serve for Bit Rate Agile (BRA) signal demodulation.

A fifteenth embodiment (15) provides a Bit Rate Agile (BRA) structure comprising: a baseband signal processing

network for receiving baseband signal streams and providing cascaded Bit Rate Agile (BRA) Time Constrained Signal (TCS) response and Long Response (LR) filtered in phase and quadrature phase baseband signals; a Quadrature Modulator serving to quadrature modulate the cascaded Time Constrained Signal (TCS) response and Long Response (LR) filtered in phase and quadrature phase baseband signals; an interface transmitter port to provide the quadrature modulated signal to the transmission medium; an interface receiver port to provide connection of the the filtered quadrature modulated signal to the demodulator; and a demodulator structure to serve for signal demodulation having Bit Rate Agile (BRA) demodulation filters Mis-Matched (MM) to that of the modulator filters.

A sixteenth embodiment (16) provides a Bit Rate Agile (BRA) structure comprising: a input port for receiving input data; a splitter having an input coupled to the input port, and serving to split the input data into baseband signal streams; a baseband signal processing network for receiving the baseband signal streams and providing cascaded Time Constrained Signal (TCS) response and Long Response (LR) filtered in phase and quadrature phase baseband signals; a Quadrature Modulator serving to quadrature modulate the Time Constrained Signal (TCS) response and Long Response (LR) filtered in phase and quadrature phase baseband signals; a transmit amplifier to provide the quadrature modulated signal to the transmission medium; an interface receiver port to provide connection of the the filtered quadrature modulated signal to the demodulator; and a demodulator structure to serve for Bit Rate Agile (BRA) signal demodulation.

A seventeenth embodiment (17) provides a structure comprising: an input port for receiving baseband signals; a baseband signal processing network for receiving the baseband signals and providing cross-correlated bit rate agile cascaded mis-matched (ACM) processed and filtered in-phase and quadrature-phase baseband signals.

A eighteenth embodiment (18) provides a signal processing, modulation, transmission, signal reception and demodulation system, for Bit Rate Agile (BRA), Modulation Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) systems comprising: (a) means for input port for receiving input data; (b) splitter means serving for BRA, MFS and CS signal splitting, having an input coupled to the input port, and serving to split the input data into baseband signal streams; (c) means for BRA, MFS and CS baseband signal processing; (d) means for receiving the baseband signal stream and providing for BRA, MFS and CS systems changeable amounts of cross-correlation between Time Constrained Signal (TCS) response processors combined with TCS and Long Response (LR) processors; (e) means for cross-correlated processed in phase (I) and quadrature (Q) phase baseband signals for quadrature modulation to the I and Q input ports of the Quadrature Modulator (QM); (f) means for an interface unit to provide the quadrature modulated data to the transmission medium; (g) means for a receiver interface unit for connection of the received cross-correlated signal to the BRA and MFS demodulator; (h) means for BRA, MFS and CS demodulation; (i) means for post-. demodulation Mis-Matched (MM) filtering of the BRA MFS and CS demodulated signals in which the MM demodulator filters are mis-matched to that of the BRA and MFS filters.

A ninteenth embodiment (19) provides a cross-correlated signal processor comprising: (a) means for Bit Rate Agile (BRA), and Modulation-Demodulation(Modem) Format Selectable (MFS) input port for receiving input data; (b) means for providing BRA and MFS in-phase (I) and quadrature phase (Q) signals; (c) BRA and MFS means for cross-correlating a fraction of a symbol or one or more symbols of the I signal with one or more symbols of the Q signal; (d) means for implementing the BRA and MFS cross-correlated signals by analog active circuits, analog passive circuits, by digital circuits or any combination thereof; (e) means for switching in-out additional filters in the I and/or Q channels; (f) means for Quadrature modulating the I and Q signals; (g) means for Linear and/or Nonlinear amplification to provide to the antenna; (h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator; (i) a BRA and MFS quadrature demodulator; and (j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the the demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

A twentieth embodiment (20) provides a cross-correlated signal processor for Bit Rate Agile (BRA) and Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) means comprising: (a) means for providing in-phase and quadrature phase signals; (b) means for cross-correlating a fraction of a symbol or one or more than one symbol of the in-phase (I) signal with a fraction of a symbol or one or more than one symbol of the quadrature-phase (Q) signal; (c) means for generating filtered cross-correlated I and Q signals; (d) means for implementing the cross-correlated signals by analog active or passive circuits, by digital circuits or combination thereof; (e) means for providing a control circuit to select from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels; (f) means for Quadrature modulating the I and Q signals; (g) means for Linear and/or Nonlinear amplification to provide to the antenna; (h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator; (i) a BRA and MFS quadrature demodulator; (j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the the demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

A twenty-first embodiment (21) provides a Cross-correlated signal processor for Bit Rate Agile (BRA) and Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) means comprising: (a) processing means for one or more input signals and providing in-phase (I) and quadrature phase (Q) signals; (b) means for cross-correlating the in-phase and quadrature shifted signals; (c) means for generating in-phase and quadrature shifted output signals having amplitudes such that the vector sum of the output signals is approximately the same at virtually all phase angles of each bit period for one set of cross-correlation and filter parameters and the vector sum is not constant for an other set of chosen filter parameters; (d) means for quadrature modulating the in-phase and quadrature output signals, to provide a cross-correlated modulated output signal; (e) means for providing a control circuit to select from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels; (f) means for Quadrature modulating the I and Q signals; (g) means for Linear and/or Nonlinear amplification to provide to the antenna; (h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator; (i) a BRA and MFS quadrature demodulator; and (j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

A twenty-second embodiment (22) provides a cross-correlated signal processor comprising: (a) means for cross-

correlating a fraction, or one or more than one symbol synchronous and/or asynchronous time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals with signal symbols of a quadrature phase shifted signal of the in-phase signal, and providing in-phase (I) and quadrature phase (Q) shifted signals for Bit Rate Agile (BRA), cascaded mismatched (ACM) Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) processing, according to the following schedule: (i) when the in-phase channel signal is zero, the quadrature shifted signal is close to the maximum amplitude normalized to one (1); (ii) when the in-phase channel signal is non-zero, the maximum magnitude of the quadrature shifted signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$; (iii) when the quadrature channel signal is zero, the in-phase signal close to the maximum amplitude; (iv) when the quadrature channel signal is non-zero, the in-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$; (b) means for quadrature modulating the in-phase and quadrature output signals to provide a cross-correlated modulated output signal; (c) controlling means and signal selection means for BRA rate, MFS and CS processor selection and selection for Linear and/or Non-Linearly Amplified(NLA) baseband and/or of Quadrature modulated signals; (d) coupling port means to the transmission medium; (e) a receiver port for connection of the received cross-correlated signal to the BRA, MFS and CS demodulator; (f) a BRA, MFS and CS quadrature demodulator; and (g) a Mis-Matched (MM) demodulator filter set for BRA, MFS and CS in which the the demodulator filter set is MM to that of the BRA, MFS and BRA filter set of the modulator.

A twenty-third embodiment (23) provides a structure for trellis coding and decoding, of extended memory Bit Rate Agile (BRA), Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) input port for receiving input data comprising: a trellis encoder; a BRA, MFS and CS splitter having an input coupled to the input port, and serving to split the input data into baseband signal streams; a BRA, MFS and CS baseband signal processing network for receiving the baseband signal streams and providing BRA, MFS and CS in phase (I) and quadrature (Q) phase baseband signals to the I and Q input ports of the transmitter; means for baseband signal processing for receiving the baseband signal streams and providing for BRA, MFS and CS systems changeable amounts of cross-correlation; means for selectively reducing the cross-correlating factor down to zero between Time Constrained Signal (TCS) response processors combined with TCS and Long Response (LR) processors; a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator; a BRA and MFS quadrature demodulator; and a Mis-Matched (MM) BRA and MFS demodulator filter set in which the the demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

A twenty-fourth embodiment (24) provides a cross correlated quadrature architecture signal processor for producing Bit Rate Agile (BRA), cross-correlated in phase and quadrature phase signal streams for modulation by a Quadrature Modulator and transmission and for signal demodulation comprising: (a) means for receiving an input BRA signal selected from the group of binary, multi-level, and analog signals and combinations thereof; (b) filtering means of the BRA input signal; (c) BRA signal shaping means for the filtered input signal; (d) amplification means for varying the modulation index of the BRA signal, the amplifier receiving the filtered input signal and providing an amplified input signal; (e) means for BRA signal splitting for receiving the amplified input signal; (f) cross correlation means of BRA data streams; and a BRA signal processor means having an in phase and quadrature phase channel each receiving one of the cross-correlated data streams, each of the in phase and quadrature phase channel having a first delay gain filter, means for generating BRA Cosine and BRA Sine values for the in phase and quadrature phase channel data stream; (g) a BRA wave shaper and a second BRA delay gain filter, such that the signal processor provides in phase and quadrature phase cross correlated data signal processor; (h) means for quadrature modulation with a BRA modulated signal adaptable for coherent or non-coherent demodulation of the quadrature BRA Frequency Modulated (FM) signal; (i) controlling means and signal selection means for BRA rate processor selection; (j) selection means for Linear and/or Non-Linearly Amplified (NLA) baseband and/or of modulated signals coupling port means to the transmission medium; (k) receiver port means for connection of one or more received cross-correlated signals to the BRA demodulator; (l) BRA demodulator means; and (m) Mis-Matched (MM) demodulator filtering means for BRA, MFS and CS demodulation in which the the demodulator filter set is MM to that of the BRA, MFS and BRA filter set of the modulator.

A twenty-fifth embodiment (25) provides a signal processing, modulation, transmission, signal reception and demodulation system, designated as Feher's Gaussian Minimum Shift Keyed (GMSK) for Bit Rate Agile (BRA), Modulation Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) systems comprising: (a) input port for receiving input data; (b) Gaussian low-pass filter and presetable gain integrator for processing the input data and providing filtered input data; (c) a splitter having an input coupled to the input port, and serving to split the filtered input data into in phase (I) and quadrature phase (Q)channel cross coupled data streams such that the I and Q data streams are proportional in gain and phase to the input data; (d) a signal processing network for receiving the I and Q channel data streams and providing processed in phase and quadrature phase signals, the signal processing network including a signal processor for varying the modulation index for the signal processing network; (e) means for generating Cosine and Sine values for the I and Q channel BRA, MFS and CS data streams; (f) means for filtering by bit rate agile FIR or IIR or switched filter and/or other post GMSK shaping filters the signals in the I and Q channels such that the signal processor provides in phase and quadrature phase cross correlated data signals for quadrature modulation with a modulated signal suitable for amplification in linear and non-linear mode; (g) means for providing the amplified signal to the transmission port; (h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator; (i) a BRA and MFS quadrature demodulator; and (j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the the demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

A twenty-sixth embodiment (26) provides a structure comprising: a input port for receiving baseand signals; and a baseband signal processing network for receiving the baseband signals and providing cross-correlated bit rate agile Peak Limited (PL) in-phase and quadrature-phase baseband signals.

A twenty-seventh embodiment (27) provides a structure for Orthogonal Frequency Division Multiplexed (OFDM) signals comprising: a input port for receiving OFDM baseband signals; and a baseband signal processing network for

receiving the baseband signals and providing cross-correlated filtered in-phase and quadrature-phase baseband signals.

A twenty-eighth embodiment (28) provides a structure comprising: a input port for receiving Orthogonal Frequency Division Multiplexed (OFDM) baseband signals; and a baseband signal processing network for receiving the OFDM signals and providing cross-correlated filtered in-phase and quadrature-phase baseband signals.

A twenty-ninth embodiment (29) provides a structure comprising: a input port for receiving Orthogonal Frequency Division Multiplexed (OFDM) baseband signals; and a baseband signal processing network for receiving the OFDM signals and providing cross-correlated Peak Limited (PL) in-phase and quadrature-phase baseband signals.

A thirtieth embodiment (30) provides a structure comprising: an input port for receiving baseband signals; a baseband signal processing network for receiving the baseband signals and providing more than two state cross-correlated filtered in- phase and quadrature-phase baseband signals; a Quadrature Modulator serving to quadrature modulate the cross-correlated filtered in-phase and quadrature-phase baseband signals; and a transmit amplifier to provide the quadrature modulated signal to the transmission medium.

A thirty-first embodiment (31) provides a Bit Rate Agile (BRA) structure comprising: a input port for receiving single or plurality of baseband binary input signals; a baseband signal processing network for receiving the baseband binary signals and providing combined Time Constrained Signal (TCS) response and Long Response (LR) filtered multi-level in-phase and quadrature-phase baseband signals; and a Quadrature Modulator serving to quadrature modulate the Time Constrained Signal (TCS) response and Long Response (LR) filtered in-phase and quadrature-phase baseband signals; a transmit amplifier to provide the quadrature modulated signal to the transmission medium; an interface receiver port to provide connection of the the filtered quadrature modulated signal to the demodulator; and a demodulator structure to serve for signal demodulation.

A thirty-second embodiment (32) provides a structure comprising: a input port for receiving a plurality of baseband signals; a baseband signal processing network for receiving the plurality of baseband signals and providing cross-correlated filtered in-phase and quadrature-phase baseband signals to two or more quadrature modulators for quadrature modulation; a set of two or more transmit amplifiers to amplify and provide the quadrature modulated signals for RF combining; and a combiner device for RF combining of the quadrature modulated amplified signals.

A thirty-third embodiment (33) provides a structure comprising: a input port for receiving a plurality of baseband signals; a baseband signal processing network for receiving the plurality of baseband signals and providing in-phase and quadrature-phase filtered baseband signals to two or more quadrature modulators for quadrature modulation; and a set of two or more transmit amplifiers to amplify and couple the quadrature modulated amplified signals to two or more antennas.

A thirty-fourth embodiment (34) provides a structure comprising: a input port for receiving baseband signals; a baseband signal processing network for receiving and splitting the signals and for providing cross-correlated filtered in-phase and quadrature-phase baseband signals to two or more quadrature modulators for quadrature modulation; and a set of two or more transmit amplifiers to amplify and provide the quadrature modulated amplified RF signals to an antenna array.

A thirty-fifth embodiment (35) provides a structure comprising: a signal processing network for receiving and splitting signals and for providing cascaded Time Constrained Signal (TCS) response and Long Response(LR) filtered in-phase and quadrature-phase baseband signals to two or more quadrature modulators for quadrature modulation; a set of two or more transmit amplifiers to amplify and provide the quadrature modulated amplified RF signals for RF combining; and a combiner device for RF combining of the quadrature modulated amplified signals.

A thirty-sixth embodiment (36) provides a structure comprising: an interface receiver port to provide connection of received Bit Rate Agile (BRA) cross-correlated filtered quadrature modulated signal to the demodulator; and a demodulator structure to serve for signal demodulation of the signal.

A thirty-seventh embodiment (37) provides an adaptive equalizer structure comprising: an interface receiver port to provide connection of received modulated signal to the pre-demodulation adaptive equalizer; a pre-demodulation adaptive equalizer structure comprising splitter, multiplier and delay structure for generating a control signal and received modulated signal time delayed product in one branch of the splitter and coupling the signal time delayed product in one branch of the splitter and the the received modulating signal in the other branch of the splitter to a signal combiner; a signal combiner structure for combining the the delayed control signal and received modulated signal product; a demodulator structure for demodulating the combined delayed control signal and received modulated signal product; and a control signal processor for generation of and connection of the control signal to the the product multiplier circuit.

A thirty-eighth embodiment (38) provides an adaptive equalizer and switchable delay structure comprising: an interface receiver port to provide connection of received modulated signal to a plurality of splitters, amplifiers, delay elements and signal combiners for signal selection of the received modulated signal; a demodulator structure for demodulating the selected received modulated signal; and a control signal processor for generation of the control signal.

The invention further provides methods and procedures performed by the structures, devices, apparatus, and systems described herein before, as well as other embodiments incorporating combinations and subcombinations of the structures highlighted above and described herein.

All publications including patents, pending patents and reports listed or mentioned in these publications and/or in this patent/invention are herein incorporated by reference to the same extent as if each publication or report, or patent or pending patent and/or references listed in these publications, reports, patents or pending patents were specifically and individually indicated to be incorporated by reference. The invention now being fully described, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without departing from the spirit or scope of the appended claims.

What is claimed is:

1. A cross-correlated signal processor comprising:

(a) means for cross-correlating a first input signal with a second input signal to generate cross-correlated in-phase (I) and quadrature-phase (Q) output signals adapted for Bit Rate Agile (BRA), cascaded mismatched (ACM) Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) processing, the first input signal comprising a fraction or one or more than one symbol synchronous and/or

asynchronous time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals, and the second input signal comprising signal symbols of a quadrature-phase signal, the cross-correlated in-phase (I) and quadrature-phase (Q) output signals generated according to the following schedule:

(i) when the in-phase signal is zero, the cross-correlated quadrature-phase signal is close to the maximum amplitude normalized to one (1);

(ii) when the in-phase signal is non-zero, the magnitude of the cross-correlated quadrature-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$;

(iii) when the quadrature-phase signal is zero, the magnitude of the cross-correlated in-phase signal is close to the maximum amplitude; and

(iv) when the quadrature-phase channel signal is non-zero, the magnitude of the cross-correlated in-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A < 1$;

(b) means for quadrature modulating the cross-correlated in-phase and quadrature-phase output signals to provide a cross-correlated quadrature modulated output signal, the means for quadrature modulating including a BRA, MFS and BRA filter set;

(c) controller and selector means for BRA rate, MFS and CS processor selection and Linear and/or Non-Linearly Amplified (NLA) baseband and/or quadrature modulated signal selection;

(d) coupling means for coupling the cross-correlated quadrature modulated output signal to a transmission medium;

(e) a BRA, MFS and CS quadrature demodulator;

(f) a receiver port for connection of the received cross-correlated signal to the BRA, MFS and CS demodulator; and

(g) a Mis-Matched (MM) demodulator filter set for BRA, MFS and CS in which a filter set of the quadrature demodulator is mis-matched to the filter set of the means for quadrature modulating.

2. A cross-correlated signal processor comprising:

(a) a cross-correlator for cross-correlating a first input signal with a second input signal to generate cross-correlated in-phase (I) and quadrature-phase (Q) output signals adapted for Bit Rate Agile (BRA), cascaded mis-matched (ACM) Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) processing, the first input signal comprising a fraction or one or more than one symbol synchronous and/or asynchronous time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals, and the second input signal comprising signal symbols of a quadrature-phase signal, the cross-correlated in-phase (I) and quadrature-phase (Q) output signals generated according to the following schedule:

(i) when the in-phase signal is zero, the cross-correlated quadrature-phase signal is close to the maximum amplitude normalized to one (1);

(ii) when the in-phase signal is non-zero, the magnitude of the cross-correlated quadrature-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$;

(iii) when the quadrature-phase signal is zero, the magnitude of the cross-correlated in-phase signal is close to the maximum amplitude; and

(iv) when the quadrature-phase signal is non-zero, the magnitude of the cross-correlated in-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$;

(b) a signal modulator for quadrature modulating the cross-correlated in-phase (I) and quadrature-phase (Q) output signals to provide a cross-correlated quadrature modulated output signal, the signal modulator including a BRA, MFS and BRA filter set;

(c) a controller and selector for selecting: (1) at least one of or any combination of: BRA, MFS, and CS processors; (2) at least one of Linearly or Non-Linearly Amplified (NLA) baseband signals, or (3) at least one of linearly, non-linearly, or partially linearly and partially non-linearly amplified quadrature modulated signals;

(d) a first coupling for coupling the cross-correlated quadrature modulated output signal to a transmission medium;

(e) a second coupling for coupling a received cross-correlated quadrature modulated signal from the transmission medium to a receiver having a receiver port;

(f) a BRA, MFS, and CS quadrature demodulator;

(g) the receiver port for connection of the received cross-correlated quadrature modulated signal to the BRA, MFS, and CS demodulator; and

(h) a Mis-Matched (MM) demodulator filter set for BRA, MFS and CS in which the demodulator filter set is mis-matched to the BRA, MFS and BRA filter set of the signal modulator.

3. The cross-correlated signal processor of claim 2, wherein the cross-correlated signal processor is adapted to process (i) an in-phase signal component; and (ii) a quadrature-phase signal component; and

the in-phase and quadrature-phase signal components characterized in that: (i) when the in-phase signal is zero, the cross-correlated quadrature-phase signal is close to the maximum amplitude normalized to one (1); (ii) when the in-phase signal is non-zero, the magnitude of the cross-correlated quadrature-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$; (iii) when the quadrature-phase signal is zero, the magnitude of the cross-correlated in-phase signal is close to the maximum amplitude; and (iv) when the quadrature-phase channel signal is non-zero, the magnitude of the cross-correlated in-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$.

4. A bit-rate agile (BRA) and modem format and code selectable signal pair comprising:

an in-phase cross-correlated channel signal component adapted for BRA, cascaded mis-matched (ACM) Modulation-Demodulation (Modem) Selectable (MFS) and Code Selectable (CS) processing; and

a quadrature-phase cross-correlated channel signal component adapted for BRA, cascaded mis-matched (ACM) Modulation-Demodulation (Modem) Selectable (MFS) and Code Selectable (CS) processing;

the in-phase and quadrature-phase cross-correlated channel signals characterized in that:

(i) when the in-phase signal is zero, the cross-correlated quadrature-phase signal is close to the maximum amplitude normalized to one (1); (ii) when the in-phase signal is non-zero, the magnitude of the cross-correlated quadrature-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$; (iii) when the quadrature-phase signal is zero, the magnitude of the cross-correlated in-phase signal is close to the maximum amplitude; and (iv) when the quadrature-phase channel signal is non-zero, the magnitude of

the cross-correlated in-phase signal is reduced from 1 (normalized) to A, where $0 \leqq A \leqq 1$; and

the bit-rate agile (BRA) cross-correlated in-phase and quadrature-phase channel signal components are derived from at least one input signal stream as a fraction of a symbol or from one or more than one symbol as a time constrained signal (TCS) response and cascaded long response (LR) filtered signals.

* * * * *

US006598232B1

(12) **United States Patent**
McAlear

(10) **Patent No.: US 6,598,232 B1**
(45) **Date of Patent: Jul. 22, 2003**

(54) **HYBRID AMPLIFIER-REGENERATOR FOR OPTIMIZING CABLE NETWORK TRANSMISSIONS**

(75) Inventor: **James Allan McAlear**, Stittsville (CA)

(73) Assignee: **Nortel Networks Limited**, St. Laurent (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/189,021**

(22) Filed: **Nov. 10, 1998**

(51) **Int. Cl.**[7] **H04N 7/173**

(52) **U.S. Cl.** **725/126**; 725/118; 725/121; 725/127; 455/15; 375/211; 370/486; 370/487; 370/490

(58) **Field of Search** 725/118, 121, 725/124–129, 111; 455/14, 20, 15; 375/211, 213, 214; 370/486, 487, 490; H04N 7/173

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,775,984	A	10/1988	Jaffre et al.	375/17
4,876,695	A	10/1989	Witters et al.	375/3
5,050,188	A *	9/1991	Dirr	375/260
5,485,630	A *	1/1996	Lee et al.	725/105
5,499,047	A *	3/1996	Terry et al.	370/486
5,719,872	A *	2/1998	Dubberly et al.	370/487
5,765,097	A *	6/1998	Dail	725/125
5,771,224	A *	6/1998	Seki et al.	370/206
5,815,794	A *	9/1998	Williams	725/106
5,878,325	A *	3/1999	Dail	725/125
6,078,950	A *	6/2000	Heidemann et al.	370/447

FOREIGN PATENT DOCUMENTS

WO	WO9701906	1/1997

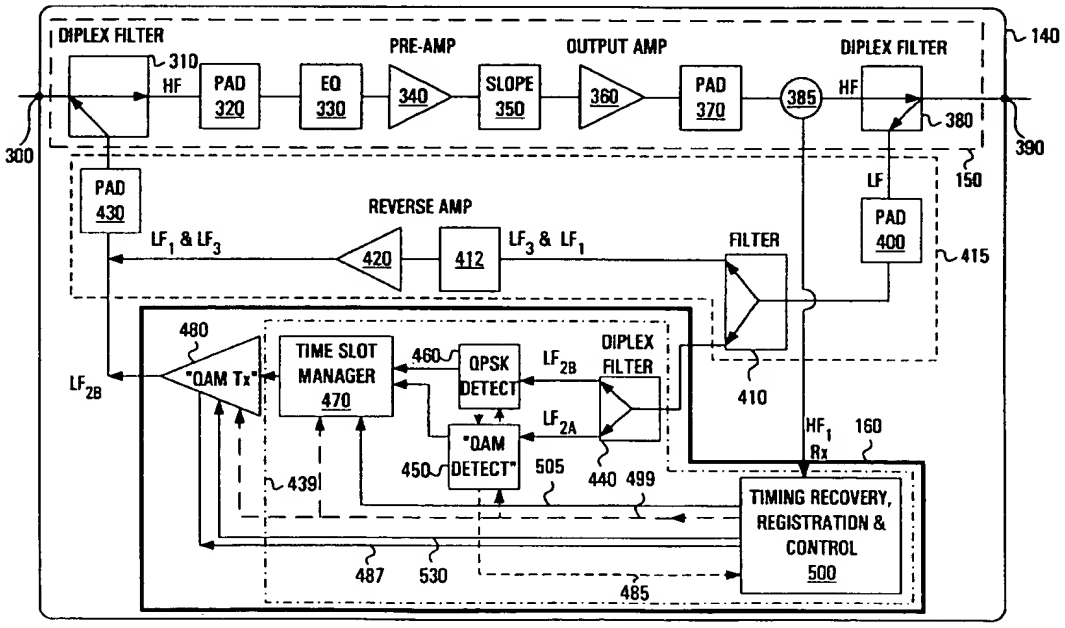
* cited by examiner

Primary Examiner—Vivek Srivastava
Assistant Examiner—Jason Salce

(57) **ABSTRACT**

A hybrid amplifier and regenerator (HAR) device is designed for use in a communications network for carrying downstream traffic in a forward frequency band and for carrying upstream traffic in a reverse frequency band spaced from the forward frequency band and below the forward frequency band. The hybrid amplifier and regenerator (HAR) device comprises an analog amplifier for amplifying the downstream traffic and a digital regenerator. The digital regenerator comprises mapping circuitry for mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express band which is also part of the reverse frequency band but spaced from the at least one ramp band, and an express band transmitter for transmitting digital upstream traffic from the mapping circuitry in the at least one express band.

39 Claims, 11 Drawing Sheets



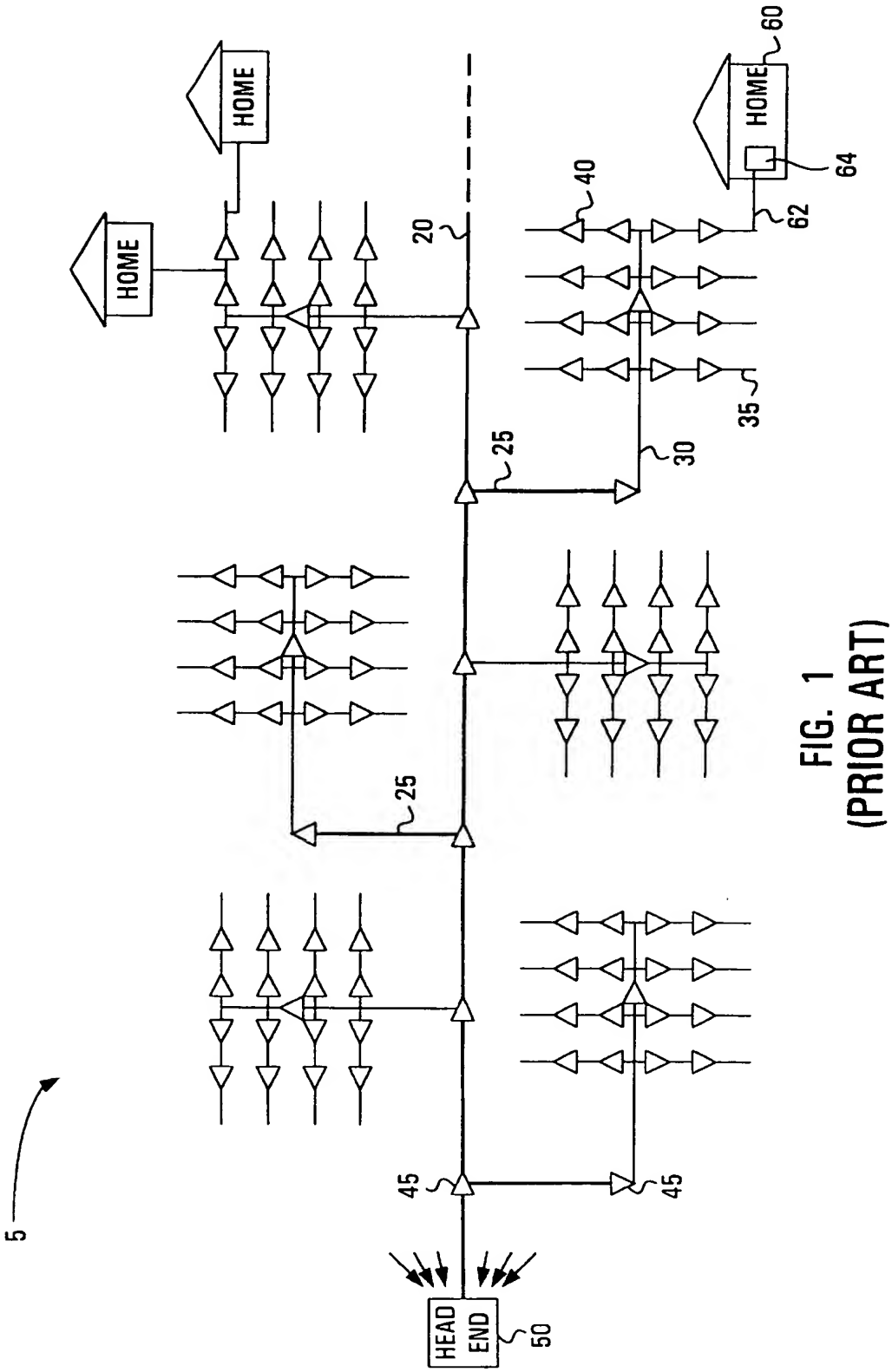


FIG. 1
(PRIOR ART)

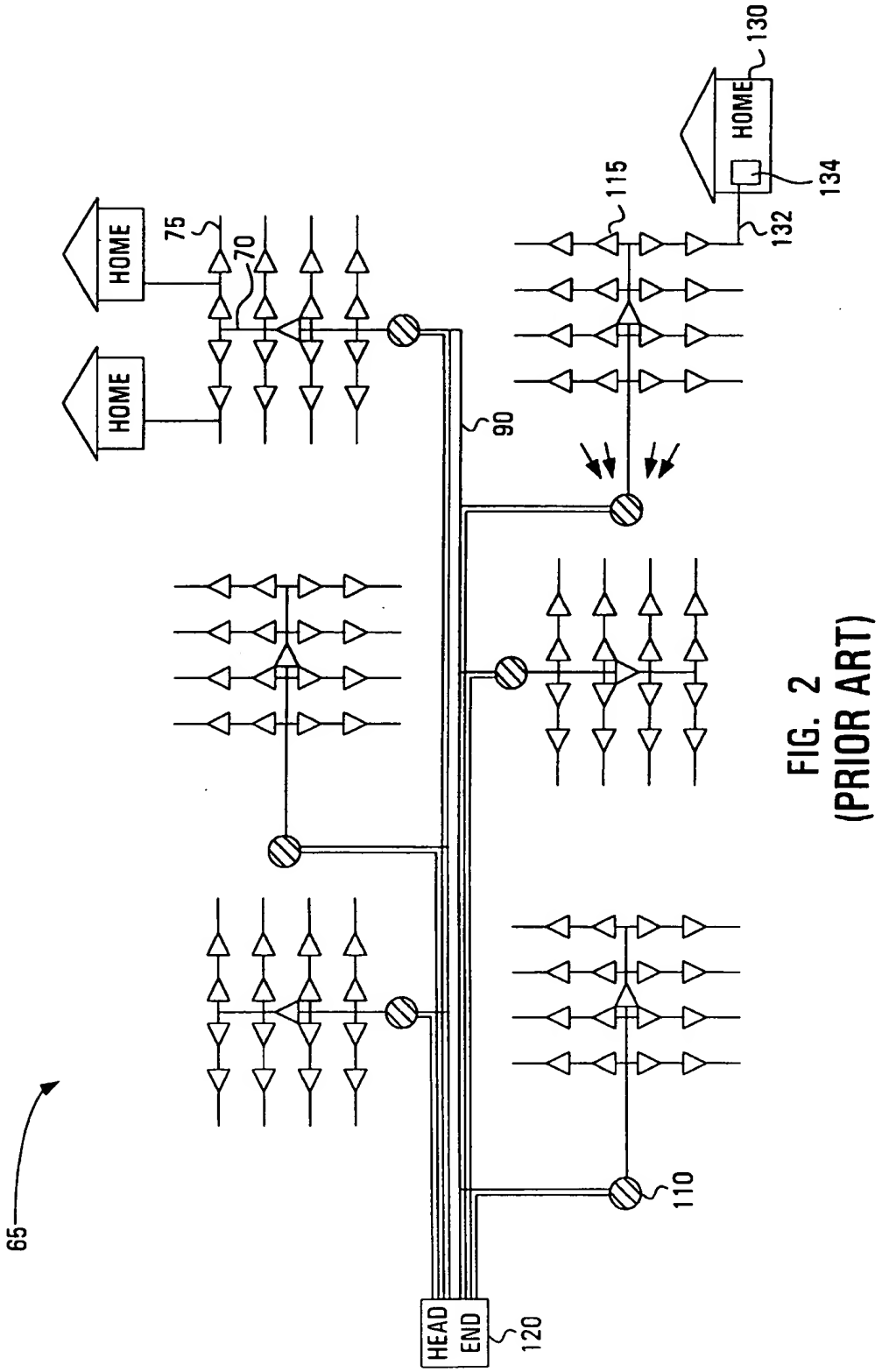


FIG. 2
(PRIOR ART)

FIG. 3A

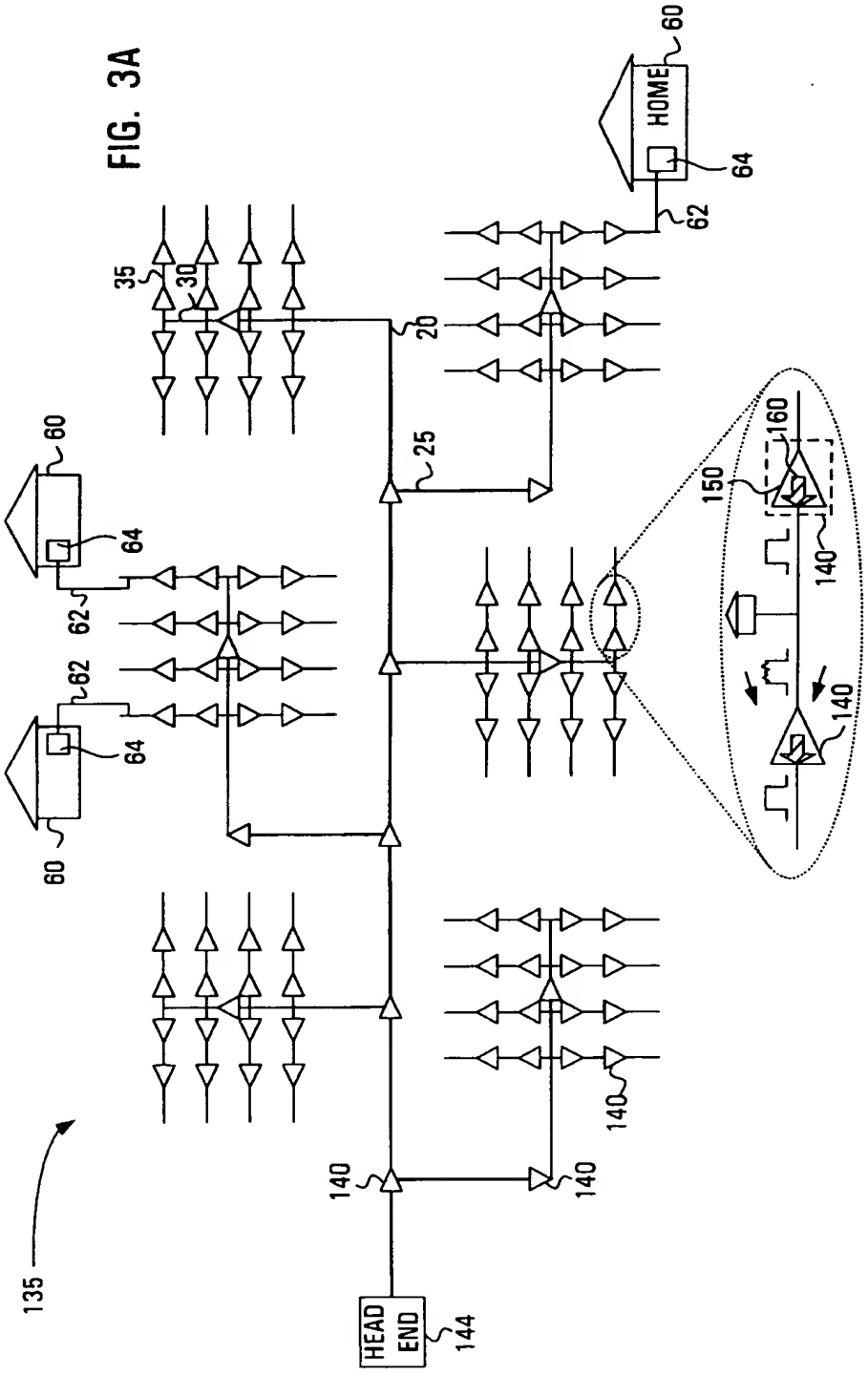

HOME
60
64
62
35
30
20
25
60
64
62
62
64
60
150
160
140
140
140
140
140
135
HEAD END
144

FIG. 3B

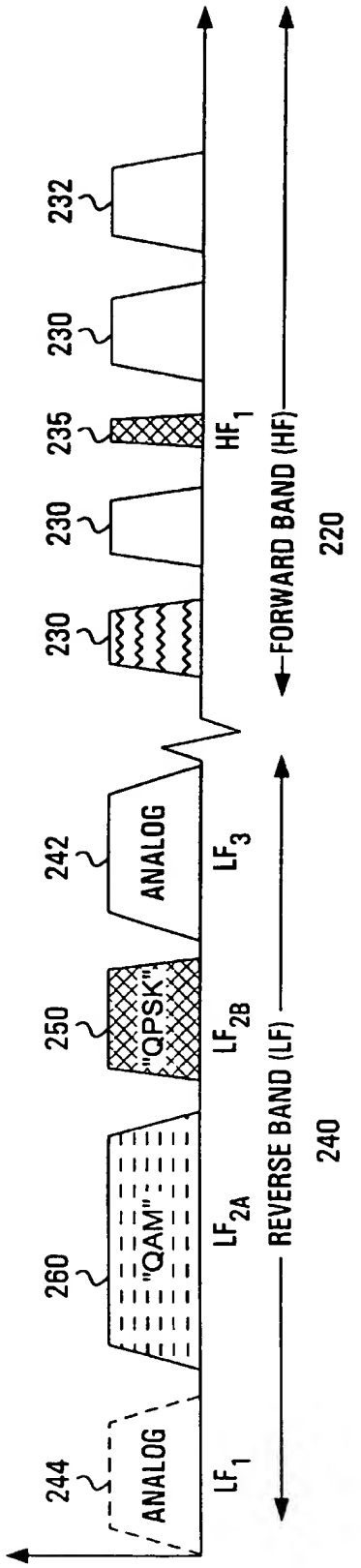

232
230
235
230
230
HF_1
FORWARD BAND (HF)
220
242
ANALOG
LF_3
250
"QPSK"
LF_{2B}
260
"QAM"
LF_{2A}
REVERSE BAND (LF)
240
244
ANALOG
LF_1

FIG. 4

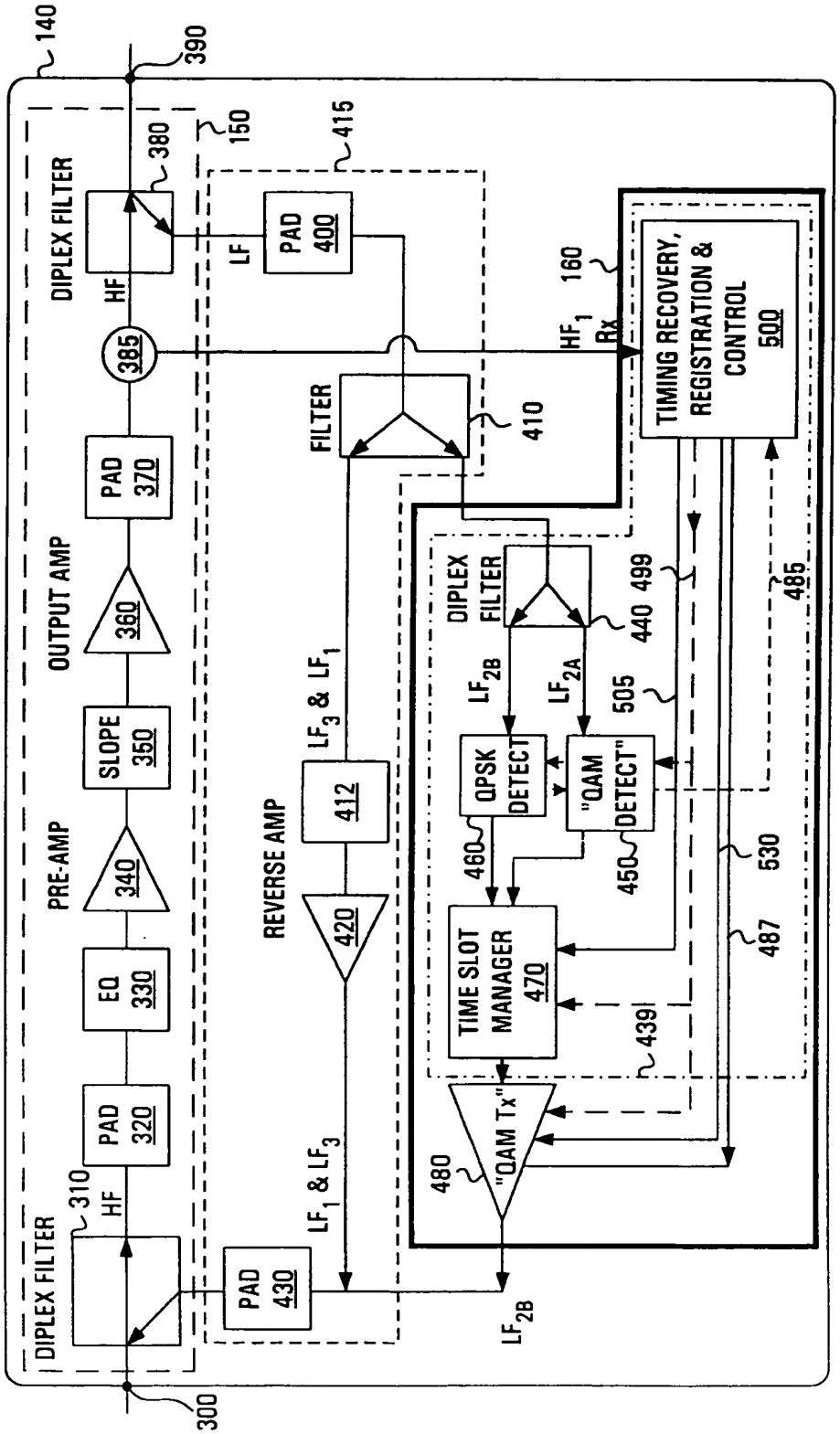

140
390
150
415
380
DIPLEX FILTER
HF
LF
PAD 400
385
FILTER
410
HF1 Rx
160
TIMING RECOVERY, REGISTRATION & CONTROL 500
PAD 370
OUTPUT AMP
360
SLOPE 350
PRE-AMP
340
EQ 330
PAD 320
310
HF
DIPLEX FILTER
PAD 430
LF1 & LF3
LF3 & LF1
412
REVERSE AMP
420
DIPLEX FILTER
440
499
485
LF2B
LF2A
505
QPSK DETECT
"QAM DETECT"
460
450
530
TIME SLOT MANAGER 470
487
439
"QAM Tx"
480
LF2B
300

FIG. 5

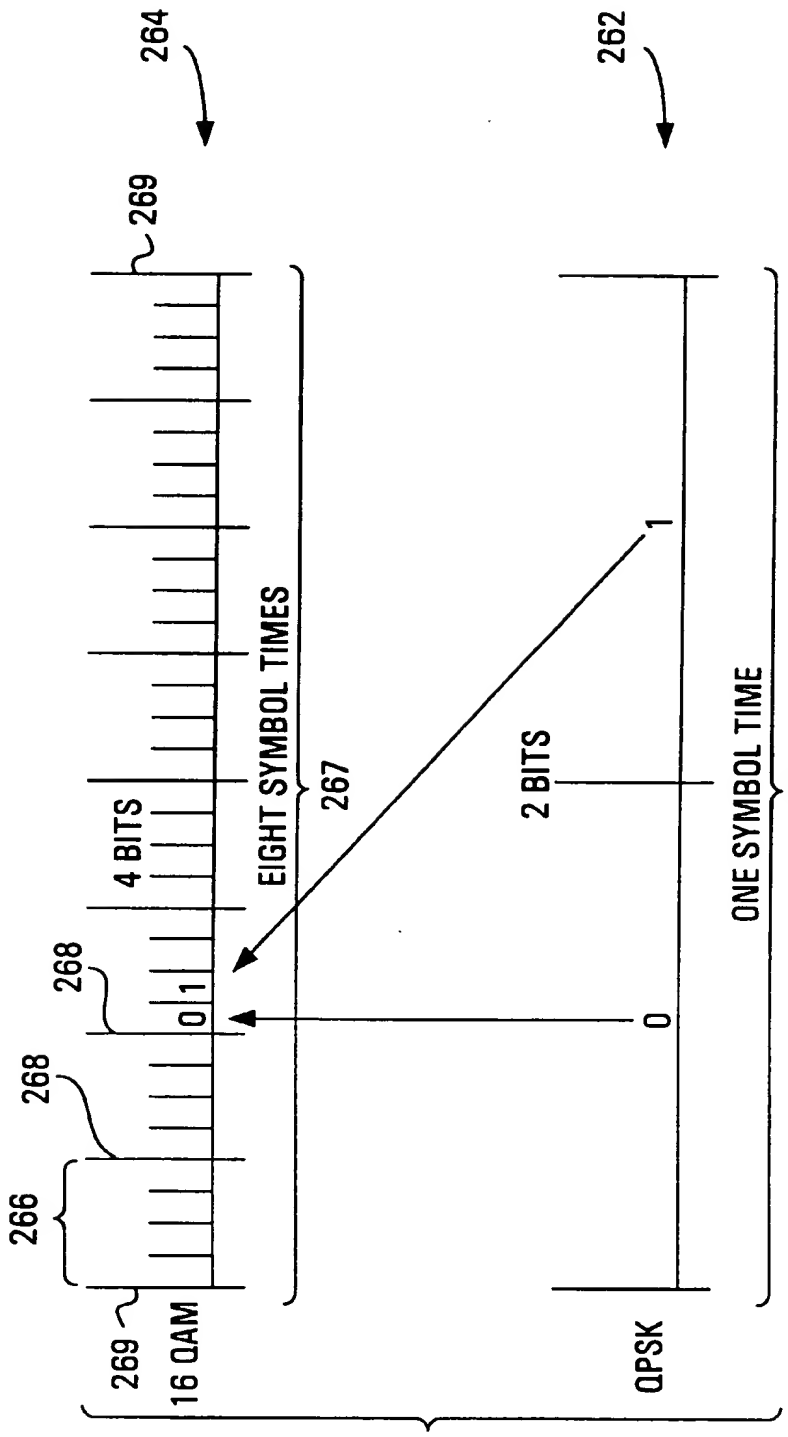

264
262
269
EIGHT SYMBOL TIMES
267
4 BITS
2 BITS
ONE SYMBOL TIME
263
268
268
266
1
0
1
0
269
16 QAM
QPSK

FIG. 6

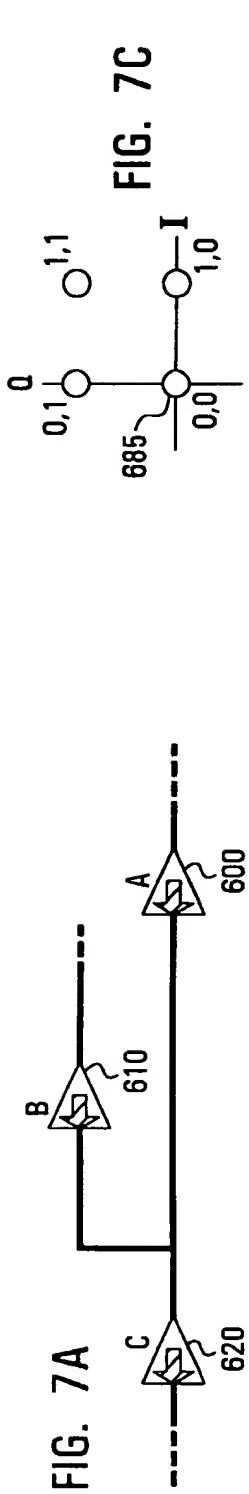


FIG. 7A

FIG. 7C

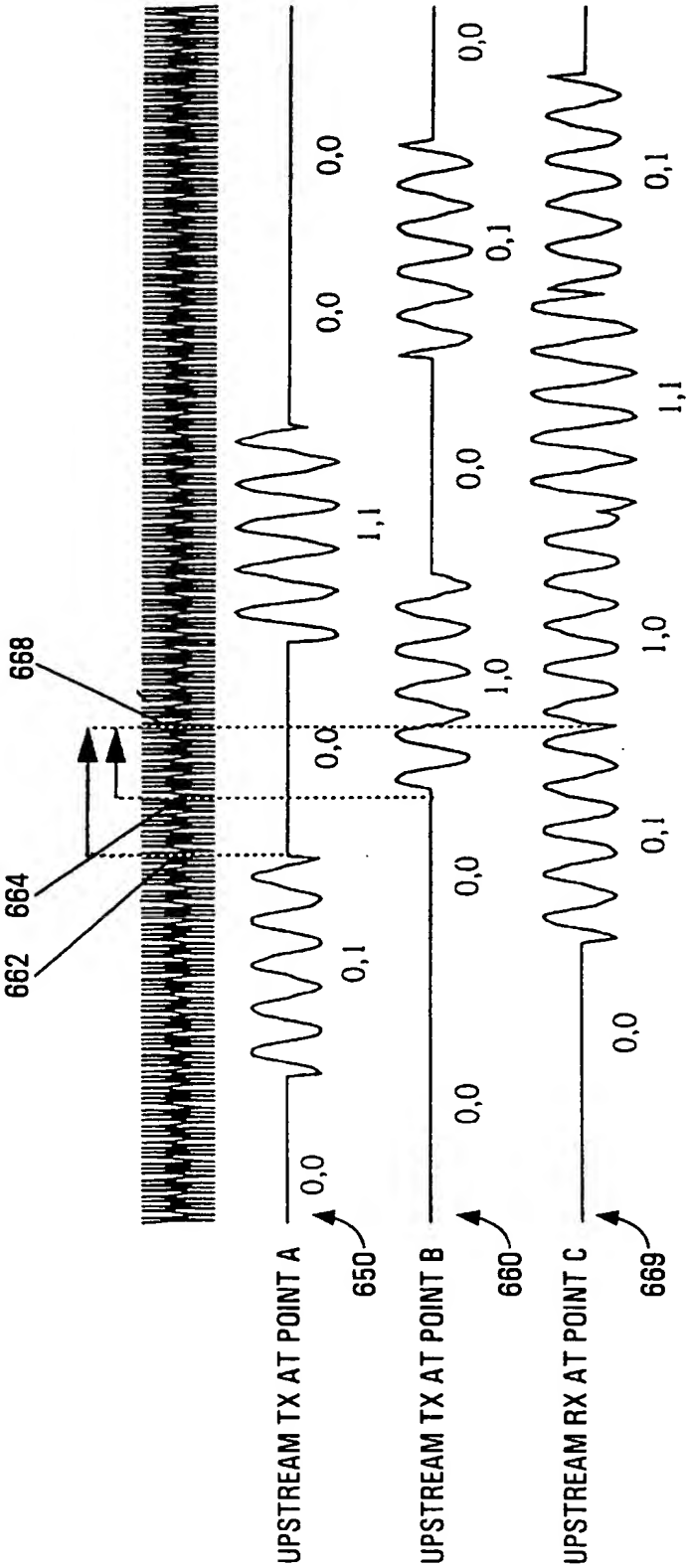


FIG. 7B

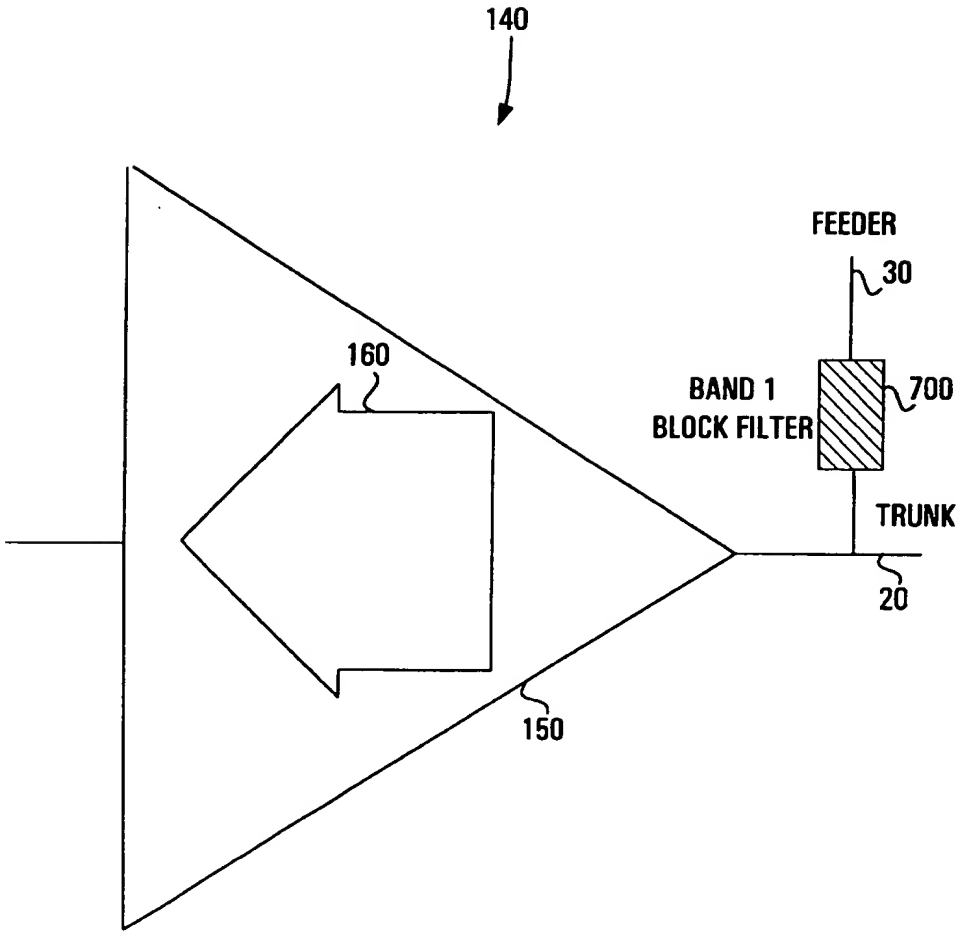


FIG. 8

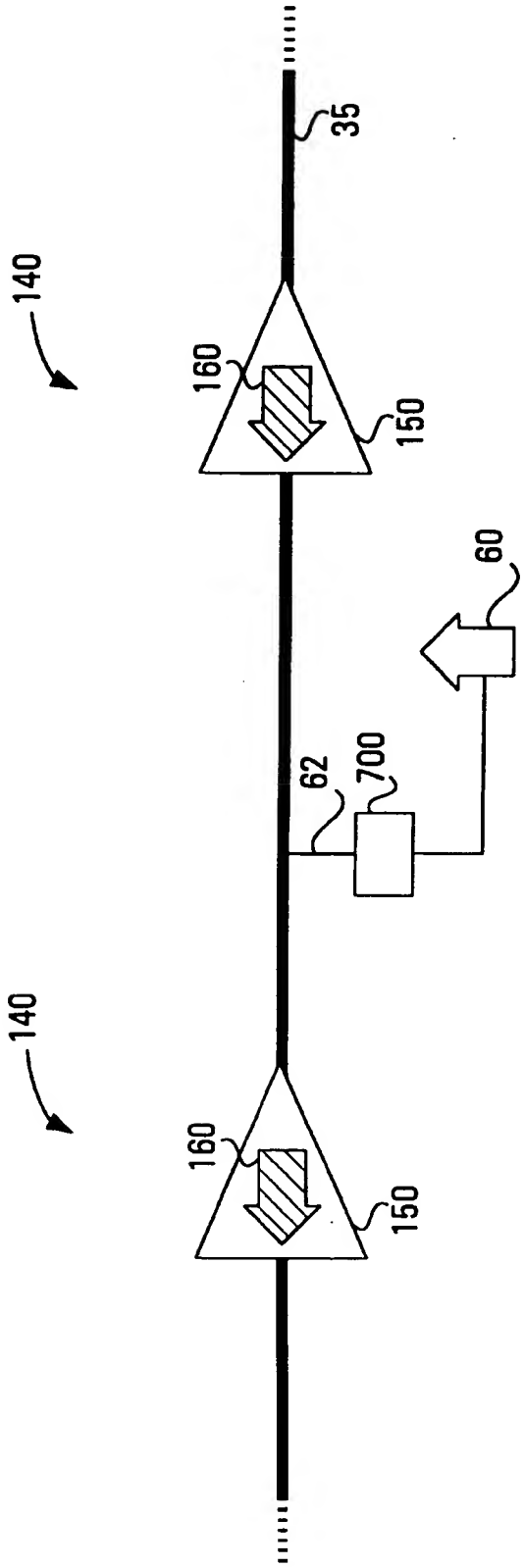


FIG. 9

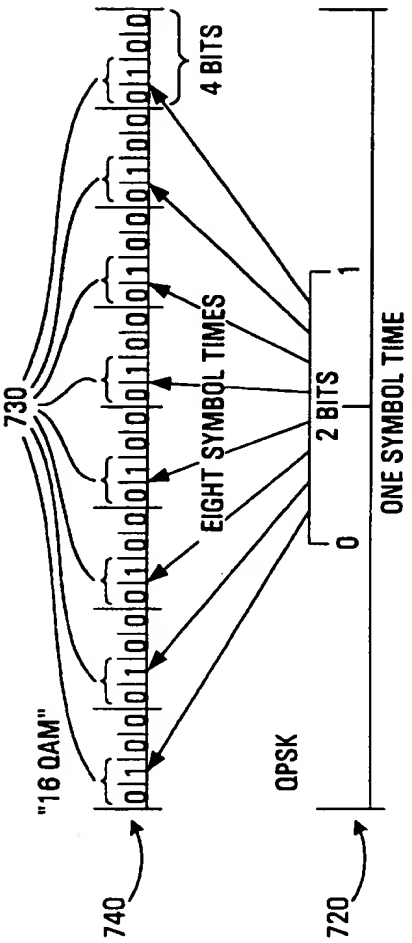

730
"16 QAM"
4 BITS
EIGHT SYMBOL TIMES
740
QPSK
2 BITS
1
0
ONE SYMBOL TIME
720

FIG. 10

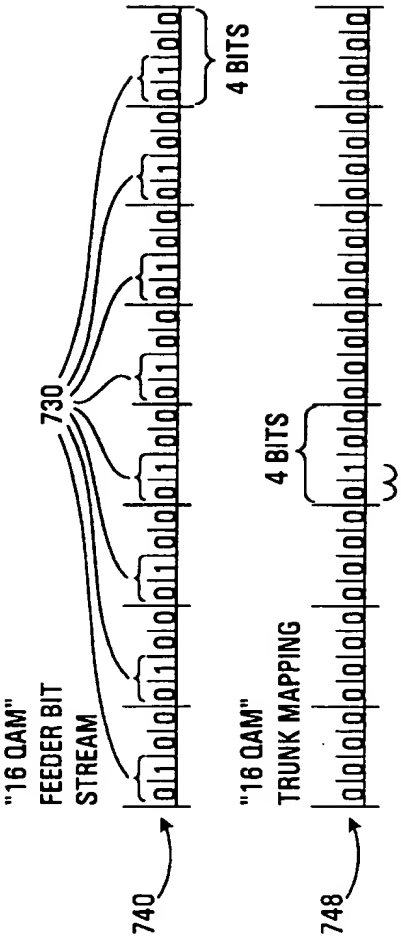

730
"16 QAM"
FEEDER BIT
STREAM
4 BITS
740
"16 QAM"
TRUNK MAPPING
4 BITS
745
748

FIG. 11

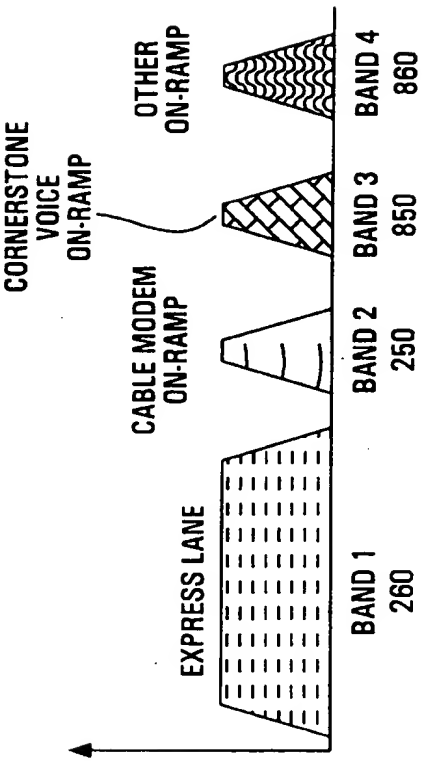

CORNERSTONE VOICE ON-RAMP
OTHER ON-RAMP
CABLE MODEM ON-RAMP
EXPRESS LANE
BAND 1 260
BAND 2 250
BAND 3 850
BAND 4 860

FIG. 12

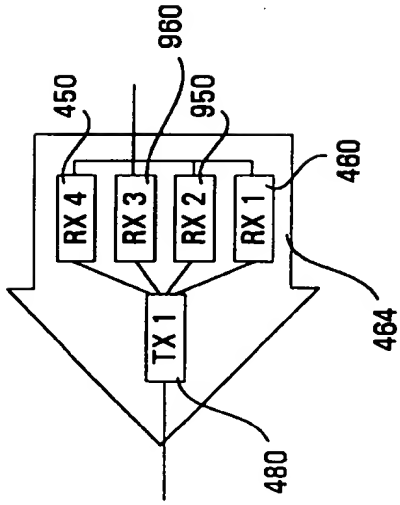

450
960
950
460
RX 4
RX 3
RX 2
RX 1
TX 1
464
480

FIG. 13

HYBRID AMPLIFIER-REGENERATOR FOR OPTIMIZING CABLE NETWORK TRANSMISSIONS

FIELD OF THE INVENTION

The present invention relates to cable television communication networks and, in particular, to optimizing upstream transmissions in such networks.

BACKGROUND OF THE INVENTION

Cable networks, sometimes referred to as CATV (community antenna TV) networks, serving residential and business premises not only provide a medium for the delivery of audio and video traffic (e.g. television and radio) for which these networks were originally designed but also provide a medium for the delivery of new services such as telephony, Internet, multimedia and data services. The new services can provide the cable system provider with an additional source of revenue.

Originally, many cable networks were designed to carry audio and video traffic (e.g. television and radio) only downstream from a cable system provider to cable subscribers. Today, many of the new services, such as telephony, require the cable network not only to carry traffic downstream from the cable system provider to the cable subscribers (downstream traffic) but also to carry traffic upstream from the cable subscribers to the cable system provider (upstream traffic). However, as shown in FIG. 1, conventional cable networks are typically implemented as a large analog bus, with analog amplifiers located along coaxial cable to boost signals where required. Since all upstream traffic typically accumulates at a single receiver point at the cable system provider, typically called the system head end, a particular problem that has been experienced is the cumulative effect of amplifier generated noise and signal distortion from the analog amplifiers on the upstream traffic. Moreover, another problem that has been experienced with the upstream traffic is the cumulative effect of ingress noise appearing at the system head end from spurious sources such as noise from cable subscriber equipment. A catastrophic ingress of noise from even a single cable subscriber can prevent any reliable upstream traffic from other cable subscribers. It is typically very difficult for a cable network provider to reduce ingress noise introduced from cable subscribers since the ingress noise is often introduced somewhere inside the premises of the cable subscribers. Other sources of ingress noise include noise from amateur radio (HAM) operators operating near the cable (CATV) network. Noise from amateur radio operators typically enters the cable (CATV) network at a point or points in the coaxial cable where the shield of the coaxial cable has been compromised. The cumulative effect of the amplifier generated noise and signal distortion and the ingress noise limits the capacity and reliability of the cable (CATV) network to carry upstream traffic.

To,minimize the problems identified above, persons skilled in the art have used hybrid fibre-coax (HFC) architectures for cable networks. Fibre optic cable is used on a trunk from a system head end to various fibre nodes. Coaxial cable is connected from the fibre nodes to a plurality of cable subscribers. Analog amplifiers are used on the coaxial cable to boost the downstream traffic and the upstream traffic. The analog amplifiers often introduce amplifier generated noise and signal distortion on the upstream traffic and the downstream traffic. The amplifier generated noise and signal distortion and any ingress noise from spurious sources (typically from the cable subscribers) all converge and accumulate at the respective fibre node. Finally, all the amplifier generated noise and signal distortion introduced by the analog amplifiers and all the ingress noise converge and accumulate at the system head end (along with all the upstream traffic).

With a hybrid fibre-coax (HFC) architecture, very little ingress noise is picked up by the trunks. However, since much of the ingress noise originates at or near the cable subscribers, much of the ingress noise is not fundamentally reduced as compared with a conventional cable network using only coaxial cable, although improvements are realized since all the amplifier generated noise and signal distortion from the analog amplifiers and the ingress noise is divided over multiple fibre nodes. The cumulative effect of the amplifier generated noise and signal distortion and the ingress noise on the system head end limits the reliability and capacity of the conventional cable network using the hybrid fibre-coax (HFC) architecture to carry upstream traffic.

In order to minimize the problems identified above, persons skilled in the art have proposed that the upstream traffic be sent using digital signals and that digital regenerators be used typically at each analog amplifier stage. The digital regenerators regenerate the digital signals and help clean out noise. The use of digital regenerators allow for much higher transmission capacity and reliability. PCT patent publication WO97/01906, published on Jan. 16, 1997, discloses the use of digital regenerators to regenerate and reduce noise on upstream traffic carried outside the recommended bandwidth of coaxial cable used in a conventional cable network. Persons skilled in the art have also attempted to address the above noted problems by using relatively costly, noise immune modulation techniques on the upstream traffic e.g. Code Division Multiplex Access (CDMA) techniques.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an improved hybrid amplifier and regenerator (HAR) device, an improved digital regenerator, an improved communication network, a method for carrying downstream traffic and upstream traffic in a communications network, and a method for processing digital upstream traffic in a digital regenerator in which the above mentioned problems are obviated or mitigated.

In accordance with one aspect of the present invention there is provided a hybrid amplifier and regenerator (HAR) device for use in a communications network for carrying downstream traffic in a forward frequency band and for carrying digital upstream traffic in a reverse frequency band spaced from the forward frequency band. The hybrid amplifier and regenerator (HAR) device comprises an analog amplifier for amplifying the downstream traffic and a digital regenerator. The digital regenerator comprises mapping circuitry for mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express band which is also part of the reverse frequency band but spaced from the at least one ramp band, and an express band transmitter for transmitting digital upstream traffic from the mapping circuitry in the at least one express band.

In accordance with another aspect of the present invention there is provided a digital regenerator for use in a hybrid amplifier and regenerator (HAR) device. The digital regen-

erator comprises mapping circuitry for mapping digital upstream traffic carried in at least one ramp band which is part of the reverse band to digital upstream traffic carried in at least one express band which is also part of the reverse band but spaced from the at least one ramp band, and an express band transmitter for transmitting digital upstream traffic from the mapping circuitry in the at least one express band.

In accordance with another aspect of the present invention there is provided a communications network for carrying downstream traffic from a system head end to a plurality of cable subscribers within a forward frequency band, and for carrying digital upstream traffic from the plurality of cable subscribers to the system head end in a reverse frequency band which is spaced from the forward frequency band. The communications network comprises transmission means for interconnecting the system head end and the plurality of cable subscribers. The communications network further comprises a plurality of hybrid amplifier and regenerator (HAR) devices located at spaced intervals along the transmission means. Each hybrid amplifier and regenerator (HAR) device comprises amplification circuitry for amplifying said downstream traffic and a digital regenerator. Thee digital regenerator comprises mapping circuitry for mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express band which is also part of the reverse frequency band but spaced from the at least one ramp band, and an express band transmitter for transmitting digital upstream traffic from the mapping circuitry in the at least one express band. The communications network further comprises cable modems for receiving the downstream traffic for the cable subscribers and for sending the digital upstream traffic from the cable subscribers in the ramp bands.

In accordance with another aspect of the present invention there is provided a method for carrying in a communications network downstream traffic in a forward frequency band and digital upstream traffic in a reverse frequency band which is spaced from the forward frequency band. The method comprises amplifying and transmitting said downstream traffic in the forward frequency band, mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express bands which is also part of the reverse frequency band but spaced from the at least one ramp band, and transmitting digital upstream traffic in the at least one express band.

In accordance with another aspect of the present invention there is provided a method for processing digital upstream traffic in a digital regenerator. The method comprises mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express band which is also part of the reverse frequency band but spaced from the at least one ramp band, and transmitting digital upstream traffic in the at least one express band.

In accordance with another aspect of the present invention there is provided a hybrid amplifier and regenerator (HAR) device for use in a communications network for carrying downstream traffic in a forward frequency band and for carrying digital upstream traffic in a reverse frequency band spaced from the forward frequency band. The hybrid amplifier and regenerator (HAR) device comprises an analog amplifier for amplifying said downstream traffic, and a digital regenerator. The digital regenerator comprises mapping circuitry for mapping digital upstream traffic carried in a ramp band which is part of the reverse frequency band to a plurality of virtual channels carried in an express band which is also part of the reverse frequency band but spaced from the ramp band, and an express band transmitter for transmitting the virtual channels from the mapping circuitry in the express band.

In accordance with another aspect of the present invention there is provided a hybrid amplifier and regenerator (HAR) device for use in a communications network for carrying downstream traffic in a forward frequency band and for carrying digital upstream traffic in a reverse frequency band spaced from the forward frequency band. The hybrid amplifier and regenerator. (HAR) device comprises an analog amplifier for amplifying said downstream traffic, and a digital regenerator. The digital regenerator comprises mapping circuitry for mapping digital upstream traffic carried in a plurality of virtual channels in an express band which is part of the reverse frequency band to a single virtual channel in the express band, and an express band transmitter for transmitting the single virtual channel from the mapping circuitry in the express band.

In accordance with another aspect of the present invention there is provided a digital regenerator for use in a hybrid amplifier and regenerator (HAR) device. The digital regenerator comprises mapping circuitry for mapping digital upstream traffic carried in a ramp band which is part of the reverse frequency band to a plurality of virtual channels carried in an express band which is also part of the reverse frequency band but spaced from the ramp band, and an express band transmitter for transmitting the virtual channels from the mapping circuitry in the express band.

In accordance with another aspect of the present invention there is provided a digital regenerator for use in a hybrid amplifier and regenerator (HAR) device. The digital regenerator comprises mapping circuitry for mapping digital upstream traffic carried in a plurality of virtual channels in an express band which is part of the reverse frequency band to a single virtual channel in the express band, and an express band transmitter for transmitting the single virtual channel from the mapping circuitry in the express band.

In accordance with another aspect of the present invention there is provided a method for multiplexing a plurality of express band transmissions, each express band transmission having a duration, from a plurality of respective downstream hybrid amplifier and regenerator (HAR) devices at an upstream hybrid amplifier and regenerator (HAR) device in the communications network. The method comprises determining a start time for each express band transmission which ensures that the express band transmissions will arrive at the upstream hybrid amplifier and regenerator (HAR) device without interfering with each other; and, beginning each express band transmission from each respective downstream hybrid amplifier and regenerator (HAR) device at each respective start time.

BRIEF DESCRIPTION OF THE DRAWINGS

A detailed description of the preferred embodiments is provided below with reference to the following drawings, in which:

FIG. 1 is an network architecture diagram showing a conventional cable (CATV) network using coaxial cable;

FIG. 2 is a network architecture diagram showing a conventional cable (CATV) network using a hybrid fibre-coax (HFC) architecture;

FIG. 3A is a network architecture diagram of cable (CATV) network in accordance with a preferred embodiment of the present invention;

FIG. 3B is simplified block diagram of a hybrid amplifier and regenerator device;

FIG. 4 is a frequency spectrum plan showing, inter alia, the ramp band and express band used in a preferred embodiment of the present invention;

FIG. 5 is a block diagram of a hybrid amplifier and regenerator (HAR) device used in a preferred embodiment of the present invention;

FIG. 6 is a diagram showing the mapping from the ramp band to the express band used in a preferred embodiment of the present invention;

FIG. 7A is a diagram showing a portion of a cable (CATV) network in which upstream traffic from two hybrid amplifier and regenerator (HAR) devices converge on one hybrid amplifier and regenerator (HAR) device;

FIG. 7B is a diagram showing the distributed multiplexing used in a preferred embodiment of the present invention;

FIG. 7C is a constellation diagram of a 4 Quadrature Amplitude Modulation (4 QAM) scheme;

FIG. 8 is a block diagram illustrating another preferred embodiment in which an express band block filter is placed on a feeder line near the trunk;

FIG. 9 is a block diagram illustrating another preferred embodiment in which an express band block filter is placed on a line to a cable subscriber;

FIG. 10 is a diagram showing the mapping from the ramp band into multiple virtual channels in the express band used in another preferred embodiment of the present invention;

FIG. 11 is a diagram showing the mapping from the multiple virtual channels in the express band into one virtual channel in the express band used in another preferred embodiment of the present invention;

FIG. 12 is a frequency spectrum plan showing three ramp bands and one express band used in another embodiment of the present invention;

FIG. 13 is a simplified block diagram of a digital regenerator used in the a modified type of hybrid amplifier and regenerator (HAR) device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows a conventional cable (CATV) network **5** which consists of a trunk **20**, a plurality of secondary trunks **25**, a plurality of feeder lines **30**, a plurality of secondary feeder lines **35**, a plurality of analog distribution amplifiers **40**, a plurality of trunk analog distribution amplifiers **45**, a system head end **50** located at a cable system provider, a plurality of cable subscribers **60**, a plurality of subscriber lines **62** and a plurality of subscriber equipment **64**.

The trunk **20**, the secondary trunks **25**, the feeder lines **30**, the secondary feeder lines **35** and the subscriber lines **62** use coaxial cable.

The analog distribution amplifiers (also called line extenders) **40** and the trunk analog distribution amplifiers **45** have a plurality of amplifier gain levels used to adjust the amount of amplification of each analog distribution amplifier **40** and each trunk analog distribution amplifier **45**.

The subscriber equipment **64** is typically televisions (TV's), stereos and subscriber equipment capable of sending upstream traffic to the system head end **50** ("upstream subscriber equipment") such as pay-per-view descramblers and cable modems. The cable modems comprise first generation cable modems, second generation cable modems or both.

The secondary trunks **25** are connected to the trunk **20**. The feeder lines **30** are typically connected to the secondary trunks **25** but may be connected directly to the trunk **20**. The secondary feeder lines **35** are connected to the feeder lines **30**. The subscriber lines **62** connect the cable subscribers **60** typically to the feeder lines **30** and the secondary feeder lines **35**. Cable subscribers **60** are not typically connected to the trunk **20** or to the secondary trunks **25** (via the subscriber lines **62**) except in some rural applications. The subscriber lines **62** are connected to the subscriber equipment **64**.

The conventional cable (CATV) network **5** is primarily used to carry audio and video traffic (e.g. radio and television) using typically analog signals (but digital signals may be used) from the system head end **50** to the cable subscribers **60**. The audio and video traffic is carried from the system head end **50**, along the trunk **20**, along the secondary trunks **25**, along the feeder lines **30**, along the secondary feeder lines **35**, along the subscriber lines **62** to the subscriber equipment **64** (e.g. TV's) of the cable subscribers **60**. The system head end **50** also,sends data traffic, using either analog or digital signals, through the cable (CATV) network **5** to the upstream subscriber equipment (e.g. data traffic instructing a pay-per-view descrambler to descramble a pay-per-view channel). In addition, data traffic may be sent from the system head end **50** using either analog or digital signals to virtually any part of the conventional cable (CATV) network **5** to control and fine tune the conventional cable (CATV) network **5**. For example, the data traffic may be sent from the system head end **50** to adjust the amplifier gain level of any analog distribution amplifier **40** or any trunk analog distribution amplifier **45**. (However, it is more common that the analog distribution amplifiers **40** and the trunk analog distribution amplifiers **45** self adjust based on pre-set reference levels). Any traffic sent from the system head end **50** is typically called downstream traffic.

The conventional cable network **5** also carries traffic to the system head end **50**. For example, data traffic is carried from the upstream subscriber equipment to the system head end **50** through the cable (CATV) network **5** using either analog or digital signals (e.g. commands may be sent from the pay-per-view equipment in a subscriber's home or data traffic may be sent from the cable subscribers' **60** cable modems for Internet or other services). The data traffic is carried along the subscriber lines **62**, along the secondary feeder lines **35**, along the feeder lines **30**, along the secondary trunks **25** and along the trunk **20** to the system head end **50**. Any traffic sent to the system head end **50** is called upstream traffic.

The trunk analog distribution amplifiers **45** are used to boost the downstream traffic and the upstream traffic carried on the trunk **20** and the secondary trunks **25**. The analog distribution amplifiers **40** are used to boost the downstream traffic and the upstream traffic carried on the feeder lines **30** and the secondary feeder lines **35**. The trunk analog distribution amplifiers typically comprise a forward trunk analog amplifier (not shown) and a reverse trunk secondary analog amplifier (not shown). Similarly, the analog distribution amplifiers typically comprise a forward analog amplifier (not shown) and a reverse secondary analog amplifier (not shown). The forward trunk analog amplifier and the forward analog amplifier boost the downstream traffic. The reverse trunk secondary analog amplifier and the reverse secondary analog amplifier boost the upstream traffic.

Many conventional cable networks **5** comply with the Data-Over-Cable Interface Specification (DOCSIS) documents, (and specifically the Radio Frequency Interface

Specification SP-RFI-104-980724) published on Jul. 24, 1998 by Cable Television Laboratories Inc. ("Cable Labs"). All the data-over-cable Interface Specification Documents are incorporated by reference herein.

Unfortunately, the analog distribution amplifies **40** and the trunk analog distribution amplifiers **45** introduce amplifier generated noise and signal distortion on the upstream traffic and the downstream traffic. The amplifier generated noise and signal distortion and any ingress noise from spurious sources all converge and accumulate at the system head end **50** along with any upstream traffic. The cumulative effect of the amplifier generated noise and signal distortion and the ingress noise limit the reliability and capacity of the cable (CATV) network **5** to carry upstream traffic. The amplifier generated noise and signal distortion introduced by the analog distribution amplifiers **40** and the trunk analog distribution amplifiers **45** and the ingress noise typically do not limit nearly as much the reliability and capacity of the conventional (CATV) network **5** to carry the downstream traffic since much of the amplifier generated noise and signal distortion and the ingress noise is distributed throughout the cable (CATV) network **5**.

FIG. **2** shows another conventional cable (CATV) network **65** which consists of a plurality of feeder lines **70**, a plurality of secondary feeder lines **75**, a plurality of fibre trunks **90**, a plurality of fibre nodes **110**, a plurality of analog distribution amplifiers **115**, a system head end **120**, a plurality of cable subscribers **130**, a plurality of subscriber lines **132** and a plurality of upstream subscriber equipment **134** (such as pay-per view descramblers and cable modems).

The feeder lines **70** are typically connected to the fibre trunks **90** via the fibre nodes **110**. The secondary feeder lines **75** are connected to the feeder lines **70**. The subscriber lines **132** connect the cable subscribers **130** to the feeder lines **70** and the secondary feeder lines **75** either directly or via the upstream subscriber equipment **134**.

The fibre trunks **90** use fibre optic cable with many fibre strands within each fibre optic cable. Typically, a pair of strands are connected to each fibre node **110**. The feeder lines **70**, the secondary feeder lines **75** and the subscriber lines **132** use coaxial cable. The fibre nodes **110** are used to bridge the fibre optic cable used on the fibre trunks **90** with the coaxial cable used on the feeder lines **70**. The fibre nodes **110** convert fibre optic signals carried on the fibre optic cable into radio frequency (RF) electromagnetic signals carried on the coaxial cable and vice versa. The analog distribution amplifiers **115** have a plurality of amplifier gain levels used to adjust the amount of amplification of each analog distribution amplifier **115**.

The analog distribution amplifiers **115** typically are the same as the analog distribution amplifiers **40** shown in FIG. **1**. That is, the analog distribution amplifiers typically comprise a forward analog amplifier (not shown) and a reverse secondary analog amplifier (not shown). The forward analog amplifiers are used to boost the downstream traffic and the reverse secondary analog amplifiers are used to boost the upstream traffic carried on the feeder lines **70** and the secondary feeder lines **75**. The downstream traffic and the upstream traffic may use either analog or digital signals.

However, the analog distribution amplifiers **115** may introduce amplifier generated noise and signal distortion on the downstream traffic and the upstream traffic. In particular, the amplifier generated noise and signal distortion and any ingress noise from spurious sources all converge and accumulate at each respective fibre node **110** along with the upstream traffic. Finally, all the amplifier generated noise and signal distortion introduced by the analog distribution amplifiers **115** and all the ingress noise converge and accumulate at the system head end **120** (along with all the upstream traffic). However, very little ingress noise is picked up by the fibre trunks **90**. In addition, since the fibre trunks **90** do not have amplifiers, the amount of amplifier generated noise and signal distortion is reduced in the conventional network **65** as compared with the conventional network **5** shown in FIG. **1**. Since much of the ingress noise originates at or near the cable subscribers **130**, much of the ingress noise is not fundamentally reduced in the conventional (CATV) network **65** as compared with the conventional (CATV) network **5** shown in FIG. **1**, although improvements are realized since all the amplifier generated noise and signal distortion and all the ingress noise are divided over multiple fibre nodes **110**. The cumulative effect of the amplifier generated noise and signal distortion and the ingress noise on the system head end limits the reliability and capacity of the conventional (CATV) network **65** to carry upstream traffic.

In accordance with a preferred embodiment of the present invention, FIG. **3A** shows a cable (CATV) network **135** which is similar in configuration to cable (CATV) network **5** shown in FIG. **1**. However, the plurality of the analog distribution amplifiers **40** and the trunk analog distribution amplifiers **45** in the cable (CATV) network **5** are replaced or upgraded with a plurality of hybrid amplifier and regenerator (HAR) devices **140**. The system head end **50** is replaced or upgraded with a more sophisticated system head end—a system head end **144** (discussed in more detail later). In addition, some of the subscriber equipment **64** must be second generation cable modems (i.e. DOCSIS compliant).

Coaxial cable is used on the subscriber lines **62**, the feeder lines **30**, the secondary feeder lines **35**, the trunk **20**, the secondary trunks **25**. (Alternatively, fibre optic cable can be used on the trunk **20** and on the secondary trunks **25** in which case a plurality of fibre nodes (not shown) are also used to connect the fibre optic cable on the trunk **20** and the secondary trunks **25** with the coaxial cable used on the feeder lines **30** and the secondary feeder lines **35**. The fibre nodes convert fibre optic signals carried on the fibre optic cable into radio frequency (RF) electromagnetic signals carried on the coaxial cable and vice versa. Furthermore, when fibre optic cable is used on the trunk **20** and on the secondary trunks **25**, the hybrid amplifier and regenerator (HAR) devices **140** are no longer needed on the trunk **20** and on the secondary trunks **25**).

Referring in particular to FIG. **3B** and to FIG. **5**, each hybrid amplifier and regenerator (HAR) device **140** comprises an analog amplifier **150** (sometimes called a downstream analog amplifier), a digital regenerator **160** (sometimes called an upstream digital regenerator) and an reverse secondary analog amplifier **415**. Each analog amplifier **150** and each reverse secondary analog amplifiers **415** have a plurality of amplifier gain levels used to adjust the amount of amplification of the respective amplifier. Similarly, each digital regenerator **160** has a timing parameter and a plurality of signal levels. The timing parameters are used to ensure that the upstream traffic is sent at the correct time and phase and to ensure proper multiplexing (discussed in more detail later). The signal levels are necessary so that the level of the signal (for the upstream traffic) sent by the respective digital regenerator **160** may be adjusted.

Referring particularly to FIG. **4**, downstream traffic from the system head end **144** is carried in a forward frequency band **220** to the cable subscribers **60**. All upstream traffic to

the system head end **144** is sent in a reverse frequency band **240** which is separate and apart from the forward frequency band **220**. The forward frequency band **220** is above the reverse frequency band **240**.

The reverse frequency band **240** and the forward frequency band **220** use conventional frequency bands. In North America and other locations of the world where NTSC standards are used, the reverse frequency band **240** is typically between 5 and 42 MHZ. The forward frequency band **220** is typically between 55 and up to 750 MHZ. Alternatively, different frequency ranges can be used for the forward frequency band **220** and the reverse frequency band **240**.

The cable (CATV) network **135** carries three types of downstream traffic. The first type of downstream traffic primarily consists of audio, video, voice, data, control and other traffic for an older service or a plurality of older services such a television, pay-per-view television, radio or services using the first generation cable modems ("old cable modem based services"). An example of an old cable based service is Internet. The second type of downstream traffic primarily consists of audio, video, voice, data and other traffic for at service or a plurality of services using the second generation cable modems ("new cable modem based services"). Examples of new cable modem based services are telephony, Internet, multimedia and other data based services. The third type of downstream traffic primarily consists of data traffic used to maintain and fine tune the hybrid amplifier and regenerator (HAR) devices **140**. For example, the third type of downstream traffic may be used to adjust the power levels of the analog amplifiers **150** and the reverse secondary analog amplifiers **415** but more suitably may be used to adjust the timing parameters and the signal levels of the digital regenerators **160**. (It is more common that the analog amplifiers **150** and the reverse secondary analog amplifiers **415** self adjust based on pre-set reference levels).

Referring to FIG. **4**, the first type of downstream traffic (for the older services such as television, radio and the old cable modem based services), is typically carried in separate broadcast channels **230** or other frequency bands which are part of the forward frequency band **220**. The broadcast channels **230** and the other frequency bands are separate and apart from each other. Other than downstream traffic for the first generation cable modems, the first type of downstream traffic is typically sent to the cable subscribers **60** using analog signals (modulated on a plurality of analog carries using analog modulation techniques such as Amplitude Modulation (AM) and Frequency Modulation (FM)). Alternatively, some or all of the first type of downstream traffic for the older services can be sent using digital signals (modulated on a plurality of analog carriers using digital modulation techniques such as Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM)). The first type of downstream traffic for the first generation cable modems are typically sent using digital signals (modulated on a plurality of analog carriers using digital modulation techniques such as Quadrature Phase Shift Keying (QPSK) and 64 Quadrature Amplitude Modulation (QAM)).

The second type of downstream traffic destined to cable subscribers **60** for the new cable modem based services such as telephony, Internet, multimedia and other data services is carried in a cable modem transmission band **232** which is part of the forward band but separate and apart from the broadcast channels and the other frequency bands in the forward band **220**. Alternatively, the second type of downstream traffic destined to the cable subscribers **60** for the new cable modem based services can also be carried in the broadcast channels **230** or in the other frequency bands in the forward frequency band **220**. The second type of traffic of downstream traffic is also be used to synchronize/align the second generation cable modems in the cable (CATV) network **135**. The second general type of downstream traffic is sent using digital signals modulated on an analog carrier or a plurality of analog carriers using **64** Quadrature Amplitude Modulation (64 QAM). Alternatively, other digital modulation techniques, such as 256 Quadrature Amplitude Modulation (256 QAM) can be used. The type of modulation technique chosen depends on the type of the second generation cable modem being used. The speed of the digital second type of downstream traffic downstream traffic is between 30 and 40 Megabits per second. (Alternatively, other speeds can be used).

The third type of downstream traffic is typically sent from the system head end **144** through one or more hybrid amplifier and regenerator (HAR) devices **140**, on a downstream control and timing tone band **235**. The downstream control and timing tone band **235** is also part of the forward frequency band **220** but is separate from the broadcast channels **230**, the other frequency bands in the forward band and the cable modem transmission band **232**. The third type of downstream traffic is modulated on a downstream control and timing tone (or carrier) of a fixed frequency using Amplitude Modulation (AM) with less than 100% modulation to ensure reliable carrier recovery. Alternatively, any other analog modulation technique that does not alter the fixed frequency can be used on the downstream control and timing tone. Alternatively, a plurality of downstream control and timing tones can be used to carry the third type of downstream traffic.

The cable (CATV) network **135** carries three types of upstream traffic. The first type of upstream traffic is upstream traffic sent by the cable subscriber(s) **60** to the system head end **144** by the upstream subscriber equipment for the older services including the old cable modem based services (e.g. upstream traffic from the pay-per-view descramblers and the first generation cable modems). The first type of upstream traffic is primarily data traffic.

The second type of upstream traffic is upstream traffic sent by the cable subscriber(s) **60** using the second generation cable modems to the system head end **144** for the new cable modem based services such as telephony, Internet, multimedia and other data based services. The second type of upstream traffic primarily consists of audio, video, data and other traffic.

The third type of upstream traffic is traffic not sent by cable subscriber(s) **60** to the system head end **144**. The third type of upstream traffic primarily consists of data traffic from virtually any part of the cable (CATV) network **135** to the system head end **144** for purposes such as monitoring the performance and status of the cable (CATV) network **135** and for maintaining the cable (CATV) network **135**. For example, the third type of upstream traffic can be used to provide information to the system head end **144** for use in controlling aligning, synchronizing and fine tuning the hybrid amplifier and regenerator (HAR) devices **140**.

The first type of upstream traffic is typically carried in the cable (CATV) network **135** using digital signals modulated on an analog carrier or a plurality of analog carriers within a first general upstream band **242** and a second general upstream band **244** using FSK, PSK, QPSK or QAM. The first general upstream band **242** and the second general

upstream band **244** are separate and apart from each other. Both the first general upstream band **242** and the second general upstream band **244** are within the reverse frequency band **240**. The first general upstream band **242** is located above 30 MHZ (and is below the forward frequency band **220**). The second general upstream band **244** is located below 10 MHZ. Alternatively, one general upstream band or more than two general upstream bands can be used to carry the first type of upstream traffic. Collectively, the first general upstream band **242** and the second general upstream band **244** are called general upstream bands. Alternatively, the first general upstream band **242** and the second general upstream band **244** may be located in different parts of the reverse band **240**.

Alternatively, the first type of upstream traffic may be carried in the cable (CATV) network **135** using analog signals or may include analog signals modulated on a analog carrier or a plurality of analog carriers within the first general upstream band **242** and/or the second general upstream band **244** using analog modulation techniques such as AM or frequency. modulation (FM).

There are typically two sub-types of the second type of upstream traffic—ramp band traffic and express band traffic. The ramp band traffic is the second type of upstream traffic carried in a ramp band **250**. The ramp band **250** is part of the reverse frequency band **240**. The express band traffic is the second type of upstream traffic carried in an express band **260**. The express band **260** is also part of the reverse frequency band **240** and is in a separate frequency band either above or below the ramp band **240**. Both the ramp band **250** and the express band **260** are typically located below the first general upstream band **242** and above the second general upstream band **244**. As discussed in more detail below, the ramp band traffic from each second generation cable modem is merged or multiplexed into the express band traffic.

In North America, the ramp band **250** is between 25 MHZ and 42 MHZ and the express band **260** is between 5 MHZ and 25 MHZ. The bandwidth of the ramp band **250** and the positioning of the ramp band **250** in the frequency spectrum is determined according to the DOCSIS specifications of the second generation cable modem being used by the cable subscribers **60** to generate the ramp band traffic. Alternatively, the express band may be located in a different part of the reverse band **240**.

The ramp band traffic is carried in the cable (CATV) network **135** using digital signals modulated on a ramp band carrier using Quadrature Phase Shift Keying (QPSK). Other digital modulation techniques can be used such as Quadrature Amplitude Modulation (QAM). The ramp band carrier is an analog carrier located within the ramp band **250**. The speed of the ramp band traffic is 640 Kbits/sec. Other speeds between 320 Kbits/sec to 10 Mbits/sec can be used. A ramp band transmission is ramp band traffic modulated on the ramp band carrier.

The express band traffic is carried in the cable (CATV) network **135** in a plurality of data frames using digital signals modulated on an express band carrier using 64 quadrature amplitude modulation (64 QAM). Other digital modulation techniques can be used such as Quadrature Phase Shift Keying (QPSK) or 16 or 256 Quadrature Amplitude Modulation (16 or 256 QAM). The express band carrier is an analog carrier located within the express band **260** and is an integral sub-multiple of the downstream control and timing tone (or carrier). The speed of the express band traffic is between 10 Mbits/sec to 40 Mbits/sec. Other speeds can be used. The speed of the express band traffic is higher than the speed of the ramp band traffic. An express band transmission is express band traffic modulated on the express band. The express band traffic is carried in a plurality of virtual channels. One of the virtual channels is a maintenance channel (discussed in more detail later).

The general upstream bands (**242** and **244**) are also capable of carrying the second type of upstream traffic. For example, if the digital regenerators **160** have failed, the system head end **144** would likely bypass (or turn off) the digital regenerators **160** and instruct the second generation cable modems to transmit in the general upstream bands (**242** and **244**).

The third type of upstream traffic, typically used by the system head end **144** to control and fine tune hybrid amplifier and regenerator (HAR) devices **140** and the second generation cable modems is carried within the maintenance channel using the same modulation technique used for the other virtual channels (e.g. 64 QAM). Alternatively, the third type of upstream traffic is carried in a plurality of maintenance channels (each maintenance channel is a virtual channel in the express band). Alternatively, the third type of upstream traffic can be carried in one or more of the general upstream bands (such as the first general upstream band **242** or the second general upstream band **244**). When the third type of upstream traffic is carried in one or more of the general upstream bands, the third type of upstream traffic is typically carried using digital signals modulated on analog carriers using digital modulation techniques such as Quadrature Phase Shift Keying (QPSK) or 64 Quadrature Amplitude Modulation (64 QAM). (Alternatively, other digital modulation techniques can be used).

The upstream traffic carried to the system head end **144** using analog signals is typically called analog upstream traffic. The upstream traffic carried to the system head end **144** using digital signals is typically called digital upstream traffic. Similarly, the downstream traffic carried from the system head end **144** using analog signals is typically called analog downstream traffic. The downstream traffic carried from the system head end **144** using digital signals is typically called digital downstream traffic.

The analog amplifiers **150** in the hybrid amplifier and regenerator (HAR) devices **140** are used to boost the first, the second and the third type of downstream traffic carried on the trunk **20**, the secondary trunks **25**, the feeder lines **30** and the secondary feeder lines **35**. As mentioned earlier, the downstream traffic is sent using either analog signals or digital signals or both (i.e. analog downstream traffic and digital downstream traffic) modulated on a plurality of analog carriers.

The reverse secondary analog amplifiers **415** in the hybrid amplifier and regenerator (HAR) devices **140** are used to boost the first type of upstream traffic carried on the first general upstream band **242** and the second general upstream band **244**. As mentioned earlier the first type of upstream traffic carried on the first general upstream band **242** and the second general upstream band **244** is sent typically using digital signals (but analog signals can be used). Furthermore, the third type of upstream traffic carried on the general upstream bands, if any, is amplified typically by the reverse secondary analog amplifiers **415** in the hybrid amplifier and regenerator devices **140**.

The digital regenerators **160** in each hybrid amplifier and regenerator (HAR) device **140** are used to regenerate and transmit the third type of upstream traffic (carried in the maintenance channel of the express band **260**) and the

second type of upstream traffic to the system head end **144**. The digital regenerators **160** help reduce noise and signal distortion on the upstream traffic.

The enhanced head end **144** has reception (i.e. receivers) and transmission equipment (i.e. transmitters). The enhanced head end **144** supplements traditional head-end processing for traditional applications (such as audio and video) and that of the older services (including old cable modem based services) with processing for new cable modem based services. In particular, the enhanced head-end **144** has additional control, managing and receiving equipment for interaction with the Hybrid amplifier and regenerator (HAR) devices **140**, especially for interaction with the digital regenerators **160** within the Hybrid amplifier and regenerator (HAR) devices **140**. The control, managing and receiving equipment is able to address each Hybrid amplifier and regenerator (HAR) device **140**, control the relative phase and amplitude of the express band transmissions sent from each Hybrid amplifier and regenerator (HAR) device **140** and assign the individual ramp band traffic to a unique virtual channel in the express band. The enhanced head end **144** also demultiplexes the express band traffic into multiple ramp band traffic and demultiplexes the ramp band traffic into data traffic from each second generation cable modem. ("cable modem traffic").

The enhanced head end **144** also maintains a time slot allocation map which keeps track of time slots assigned to individual second generation cable modems. A copy of the time slot allocation map is sent by the head end **144** to all the second generation cable modems. Each second generation cable modem has a unique identifier number. Each second generation cable modem reads the time slot allocation map and in particular reads the data in the time slot allocation map corresponding to the identifier number of the respective second generation cable modem. After reading the time slop allocation map, each cable modem transmits data within its designated time slot. It should be noted that the same time slot can be reused by another second generation cable modem in a different feeder line **30** or secondary feeder line **35** of the network **135** that maps into a different virtual channel of the express band **260**. In other words, two or more second generation cable modems could be assigned to transmit at exactly the same time on the same ramp band **250** if the second generation cable modems are located in different feeder lines **30** or secondary feeder lines **35** and their respective ramp band traffic is mapped into different virtual channels of the express band **260**.

The time slot allocation map also contains the carrier frequency of the ramp band **250**, the modulation format (e.g. QPSK) and the speed (e.g. 640 Kbits/sec).

A second time slot allocation map maintains a plurality of second time slots in other bands which are part of the first general upstream band **242** or the second general upstream band **244**. The second time slots are typically assigned to first generation cable modems. However, as previously mentioned, the second time slots may also be assigned to second generation cable modems (e.g. If the digital regenerators **160** have failed, the second generation cable modems may be assigned to transmit in the general upstream bands (**242** and **244**) during the respective second time slot as specified by the second time slot allocation map).

If multiple ramp bands **250** are used (discussed in more detail later), the head end **144** keeps a frequency/time slot allocation map which keeps track of specific time slots and frequencies assigned to individual second generation cable modems.

The second generation cable modems receives the second type of downstream traffic on the downstream cable modem transmission band **232**. In particular, the second generation cable modems demodulate transmissions from the system head end **144** on the cable modem transmission band **232**. In addition, the second generation cable modems modulate the ramp band traffic on the ramp band **250** from the cable subscribers **60**. In particular, the second generation cable modems modulate the ramp band carrier with the second type of digital upstream traffic from the cable subscribers **60** using QPSK in order to generate and send the ramp band traffic (via ramp band transmissions). Any analog upstream traffic (e.g. telephony) from the cable subscribers **60** is first digitized by a plurality of conversion devices (such as an analog to digital converters (A/D converters)) external from the second generation cable modems. (Alternatively, conversion devices internal to the second generation cable modems can be used). Then, the second generation cable modems modulate the ramp band carrier with the digital upstream traffic from the conversion devices in order to generate and send the ramp band traffic. Each second generation cable modem has a timing parameter and a plurality of signal levels. In addition, each second generation cable modems can operate on a plurality of frequencies (i.e. the frequency of the ramp band carrier can be adjusted).

As mentioned earlier, each hybrid amplifier and regenerator (HAR) device **140** comprises an analog amplifier **150**, a reverse secondary analog amplifier **415**, and a digital regenerator **160**. Referring to FIG. **5**, the analog amplifier **150** comprises a diplex filter **310**, an attenuation pad **320**, an equalizer **330**, a pre-amplifier **340**, a slope compensator **350**, an output amplifier **360**, an attenuation pad **370** and a diplex filter **380**. The reverse secondary analog amplifier **415** comprises an attenuation pad **400**, a triplex filter **410**, an equalizer **412**, an analog amplifier **420** and an attenuation pad **430**. The digital regenerator **160** comprises mapping circuitry **439** and an express band transmitter **480**. It should be noted that the hybrid amplifier and regenerator (HAR) device **140** can be considered as being formed by adding a digital regenerator **160** to a conventional amplifier comprising the analog amplifier **150** and the reverse secondary analog amplifier **415**. The digital regenerator **160** can be put on a daughter board which can be connected to the conventional amplifier.

All downstream traffic from the system head end **144** enters the hybrid amplifier and regenerator (HAR) device **140** at I/O point **300** and arrives at the diplex filter **310**. The diplex filter **310** only allows the passage of downstream traffic carried in the forward frequency band **220** to the attenuation pad **320**. The attenuation pad **320** is adjusted to attenuate the downstream traffic so as to prevent the overloading of the pre-amplifier **340**. The downstream traffic is carried from the attenuation pad **320** to the equalizer **330**. Since downstream traffic carried in higher frequencies tend to lose more signal strength than downstream traffic carried in lower frequencies, the equalizers **330** helps to equalize the signal strength of the lower frequencies and the higher frequencies by attenuating the lower frequencies. The downstream traffic from the equalizer **330** is amplified by the pre-amplifier **340** and carried to the slope compensator **350**. Since the pre-amplifier **340** provides equal amplification to the higher frequencies and the lower frequencies, the slope compensator **350** helps to emphasize the signal strength of the higher frequencies by attenuating the lower frequencies. Downstream traffic from the slope compensator **350** is amplified by the amplifier **360** and carried to the attenuation pad **370**. Attenuation pad **370** is adjusted so as to attenuate

the downstream signals to help prevent overloading equipment used by a cable subscriber **60** or another hybrid amplifier and regenerator (HAR) device **140** located downstream. The downstream traffic passes through the diplex filter **380** to an input/output point **390**. At a point **385** just before the diplex filter **380**, the third type of downstream traffic carried on the downstream control and timing tone band **235** is carried to a control unit **500** (discussed in more detail below).

All upstream traffic carried in the reverse frequency band **240** enters the hybrid amplifier and regenerator (HAR) device **140** at the input/output point **390** and is separated from any downstream traffic in the forward frequency band by the diplex filter **380** and is carried to the attenuation pad **400**. The attenuation pad **400** is adjusted to attenuate the analog and digital upstream traffic so as to prevent the overloading of the digital regenerator **160** and the analog amplifier **420**. The upstream traffic is then carried to the triplex filter **410**. The triplex filter **410** separates the upstream traffic carried on the first general upstream band **242** and the second general upstream band; **244** from the traffic carried on the ramp band **250** and the express band **260**. (If either the first general upstream band, **242** or the second general upstream band **244** is not used, the triplex filter **410** is replaced with a diplex filter. The diplex filter separates the upstream traffic carried on either the first general upstream band **242** or the second general upstream band **244** from the upstream traffic carried on the ramp band **250** and the express band **260**). The upstream traffic carried on the first general upstream band **242** and the second general upstream band **244** is carried from the triplex filter **410** to the equalizer **412**. Since upstream traffic carried in higher frequencies tend to lose more signal strength than downstream traffic carried in lower frequencies, the equalizer **412** helps to equalize the signal strength of the lower frequencies and the higher frequencies by attenuating the lower frequencies. The upstream traffic is then carried from the equalizer **412** to the analog amplifier **420**. The analog amplifier **420** amplifies the analog upstream traffic. The analog upstream traffic is then carried to the attenuation pad **430**. The attenuation pad **430** is adjusted to attenuate the analog upstream traffic and the digital upstream traffic so as to prevent the overloading of any hybrid amplifier and regenerator (HAR) devices **140** upstream.

The upstream traffic carried on the ramp band **250** and the express band **260** is carried from the triplex filter **410** to the digital regenerator **160**. In particular, the upstream traffic carried on the ramp band **250** and the express band **260** is carried from the triplex filter **410** to the mapping circuitry **429**. Mapping Circuitry **439** consists of the diplex filter **440**, an express band receiver **450**, a ramp band receiver **460**, a time slot manager **470** and the control unit **500**. In particular, the upstream traffic carried on the ramp band **250** and the express band **260** is carried from the triplex filter **410** to the diplex filter **440**. The diplex filter **440** separates the upstream traffic carried on the ramp band **250** from the traffic carried on the express band **260**. The upstream traffic carried on the express band **260** and the upstream traffic carried on the ramp band **250** is carried separately to the express band receiver **450** and the ramp band receiver **460** respectively. The ramp band receiver **460** detects and converts the digital signals carried on the ramp band **250** into a ramp band Bitstream. Similarly, the express band receiver **450** detects and converts the digital signals carried on the express band **260** into an express band Bitstream. (In particular, the express band detector **450** and the ramp band detector **460** typically detect the phase and amplitude of the ramp band carrier and the express band carrier respectively in order to detect and convert the digital signals carried on the ramp band **250** and the express band **260** respectively). The upstream traffic carried in the express band **260** from the express band detector **450** and the upstream traffic carried in the ramp band **250** from the ramp band detector **460** is carried to the time slot manager **470**. The time slot manager **470** maps the ramp band traffic carried on the ramp band **250** into the express band traffic carried on the express band **260** using digital time division multiplexing (discussed in more detail later). In order to co-ordinate the digital time division multiplexing, the control unit **500** sends a time slot control signal on a time slot control line **505**. The upstream traffic carried on the express band **260** is then carried from the time slot manager **470** to the express band transmitter **480**. The express band transmitter **480** modulates the express band carrier with the express band traffic from the time slot manager **470**. The upstream traffic from the express band transmitter **480** is then carried to the attenuation pad **430**. The analog upstream traffic and the digital upstream traffic is then carried from the attenuation pad **430** through the diplex filter **310** and through the input/output point **300**.

As discussed in more detail later, for the network **135** to operate, correctly, it is necessary for each Hybrid amplifier and regenerator (HAR) device **140** to send its express band traffic at a certain phase and amplitude. If a Hybrid amplifier and regenerator (HAR) device **140** is misaligned (the misaligned HAR **140'**), the Hybrid amplifier and regenerator (HAR) device **140** upstream from the misaligned HAR **140** will receive express band traffic with an incorrect phase and/or amplitude ("a level or a phase error"). The express band detector **450** of the upstream Hybrid amplifier and regenerator (HAR) device **140** sends an error detect signal to the control unit **500** on error detect line **485**. The control unit **500** informs the system head end **144** of the level or the phase error by sending the third type of upstream traffic in the maintenance channel of the express band **260**. This upstream traffic is carried on line **487** to the express band transmitter **480**, through the attenuation pad **430**, through the diplex filter **310**, through input/output point **300**, through other hybrid amplifier and regenerator (HAR) devices **140**, if any, and finally to the system head end **144**. The system head end **144** sends the third type of downstream traffic in the downstream control and timing tone band **235** through one or more hybrid amplifier and regenerator (HAR) devices **140**, if any, to the misaligned hybrid amplifier and regenerator (HAR) device **140**. The downstream traffic sent by the system head end **144** will cause a revision of the amplitude or phase of the express band traffic sent by the misaligned hybrid amplifier and regenerator (HAR) device. This process iterates until the level or phase error is eliminated or reduced to negligible levels.

In particular, in response to the third type of downstream traffic sent by the head end **144**, the misaligned Hybrid amplifier and regenerator (HAR) device **140** changes the phase or amplitude of the express band traffic by sending a signal from the control unit **500** along an express band control line **530** to the express band transmitter **480** to adjust the amplitude or phase of the express band transmission.

As discussed later, if a hybrid amplifier and regenerator device (HAR) **140** ("the upstream HAR") detects that the digital multiplexing performed by another Hybrid amplifier and regenerator (HAR) device **140** downstream ("the downstream HAR") is incorrect, the control unit **500** in the upstream HAR **140** informs the system head end **144** of the problem by sending a third type of upstream traffic in the maintenance channel of the express band **260**. The upstream

traffic is carried on line **487** to the express band transmitter **480**, through the attenuation pad **430**, through the diplex filter **310**, through the input/output point **300**, through other hybrid amplifier and regenerator (HAR) devices **140**, if any, and finally to the system head end **144**. The system head end **144** sends the third type of downstream traffic in the downstream control and timing tone band **235** through one or more hybrid amplifier and regenerator (HAR) devices **140**, if any, to the downstream misaligned HAR **140**. The downstream traffic is received by the control unit **500** in the downstream HAR **140**. The control unit **500** sends a signal from the time slot control line **505** to the time slot manager **470** to correct the problem (as discussed in more detail later).

The downstream control and timing tone (or carrier) provides the timing reference to all the hybrid amplifier and regenerator (HAR) devices **140** in the cable (CATV) network **135** on the downstream control and timing tone band **235**. In particular, the control unit **500** in each hybrid amplifier and regenerator (HAR) device **140** has an integer divider circuit, not shown. The control unit **500** receives the downstream control and timing tone and detects and sends the timing reference into the integer divider circuit and out on clock out lines **499** to the express band detector **450**, the ramp band detector **460**, the time slot manager **470** and the express band transmitter **480**.

Similarly, if either the amplitude or frequency of the ramp band traffic received by a Hybrid amplifier and regenerator (HAR) device **140** from a second generation cable modem ("the misaligned cable modem") is incorrect ("a level or a frequency error"), the ramp band detector **460** of the HAR **140** sends an error detect signal to the control unit **500** on error detect line **485**. The control unit **500** informs the system head end **144** of the level or the frequency error by sending the third type of upstream traffic in the maintenance channel of the express band **260**. This upstream traffic is carried on line **487** to the express band transmitter **480**, through the attenuation pad **430**, through the diplex filter **310**, through input/output point **300**, through other hybrid amplifier and regenerator (HAR) devices **140**, if any, and finally to the system head end **144**. The system head end **144** sends the second type of downstream traffic in the cable modem transmission band **232** through one or more hybrid amplifier and regenerator (HAR) devices **140**, if any, to the misaligned second generation cable modem. The downstream traffic sent by the system head end **144** will cause a revision of the amplitude or frequency of the ramp band traffic. This process iterates until the level or phase error is eliminated or reduced to negligible levels.

Referring in particular to FIG. **6**, the ramp band receiver **460** in each digital regenerator **160** detects the digital signals carried in the ramp band **250** and converts them into a ramp band Bitstream **262**. The ramp band Bitstream **262** consists of a series of digital bits (i.e. either a 0 or a 1). Similarly, the express band receiver **450** in each digital regenerator **160** detects the digital signals carried in the express band **260** and converts them into an express band Bitstream **264**. The express band Bitstream **264** also consists of a series of digital bits.

As mentioned earlier, the ramp band traffic is modulated on a ramp band carrier using the QPSK modulation technique. Two bits can constitute one ramp band symbol **263** in QPSK. The express band traffic is modulated on an express band carrier using the 64 QAM modulation technique. For the sake of simplicity, FIG. **6** illustrates 16 QAM. In 16 QAM, **4** bits constitute one express band symbol **266**. Furthermore, in 16 QAM, 8 symbols constitute an express band data frame **267**. If a different modulation scheme was used, the number of bits constituting an express band symbol and the number of symbols constituting the express band data frame may be different. Each express band symbol **266** have express band symbol boundaries **268**. Similarly, each express band data frame **267** have express band data frame boundaries **269**. Each express band data frame boundary **269** is also an express band symbol boundary **268**. Similarly, each ramp band symbol **263** has ramp band symbol boundaries.

The ramp band traffic is mapped (or multiplexed) into the express band traffic by the time slot manager **470** in each digital regenerator **160**. In particular, the ramp band traffic is converted into express band traffic by mapping each ramp band symbol **263** into a precise location in each data frame of the express band Bitstream **264** using digital time division multiplexing. (Typically each ramp band symbol **263** is mapped into a portion of one of the express band symbols **266** as shown in FIG. **6**). The precise location is one of the virtual channels of the express band **260**. The resulting express band traffic is modulated on the express band carrier by the express band transmitter **480** using 64 QAM.

It should be noted that all ramp band transmissions from the second generation cable modems are transmitted in packets (in bursts) within time slots according to the time slot allocation map. Each burst packet begins with a specified preamble sequence which allows the ramp band receiver to properly acquire the carrier frequency and phase of the ramp band and to determine the symbol boundary of the first ramp band symbol. In general, some of the preamble sequence is multiplexed into the express band **260** where they can be used to detect the boundary of the first ramp band symbol in a burst packet.

In reference to the above, persons skilled in the art would appreciate that a QPSK symbol represents 2 bits, whereas a 64 QAM symbol represents 8 bits in 1/32 the duration. In other words, 32 64 QAM symbols each representing 8 bits, can be sent in the same amount of time as a single QPSK symbol representing only 2 bits. Thus, it should be clear that the data rate or the 64 QAM sequence (i.e. in the express band) is 128 (=32 [64 QAM symbols]×8 [bits/64 QAM symbol]×½ [QPSK symbol/bit]) times greater than the data rate of the QPSK sequence (i.e. in the ramp band). Thus, simply put, an express band transports upstream traffic at a substantially higher data rate as compared to any ramp band so that upstream traffic originating from a number of sources can be aggregated from multiple ramp bands into an express band.

Given, as an example for the sake of simplicity, in reference to FIG. **6** is the illustration representing the mapping from a QPSK ramp band to a 16 QAM express band. Shown in FIG. **6**, there are eight 16 QAM symbols, each representing 4 bits, sent in the same amount of time as a single QPSK symbol in the ramp band. In fact, the data from the QPSK symbols in the ramp band is mapped into the 16 QAM symbols (in reality it is preferably into 64 QAM symbols) in the express band. Again, those skilled in the art would appreciate that the mapping of data from the QPSK ramp band into the example 16 QAM express band results in a 16 fold increase in the rate at which data is transmitted.

With frequently placed regenerators in the cable (CATV) network **135**, reliable and high capacity upstream transmissions can be accomplished. Noise on the express band **260** is typically cleaned out by each regenerator provided that the noise has not generated a bit error. The upstream traffic on the express band **260** is transmitted anew on the express

band 260 by each regenerator. Furthermore, the digital time division multiplexing prevents any noise in the ramp band from affecting the upstream traffic previously mapped into the express band using digital time division multiplexing.

The hybrid amplifier and regenerator (HAR) devices 140 with the digital regenerators 160 are located in the cable (CATV) network 135 at intervals sufficiently closely spaced to overcome the attenuation of the upstream traffic and the downstream traffic. Typically, the hybrid amplifier and regenerator (HAR) devices 140 are spaced 500 to 1000 feet or less apart respectively. (It should be noted that the intervals are engineering parameters and depend on the bandwidth of the system, cable size and loss, amplifier gain, etc.).

In addition to the multiplexing which happens from the ramp band 250 to the express band 260, there is multiplexing of the digital upstream traffic on the express band 260 whenever multiple hybrid amplifier and regenerator (HAR) devices 140 transmit upstream traffic to a single hybrid amplifier and regenerator (HAR) device as shown in FIG. 7A. FIGS. 7A and 7B illustrate two upstream transmissions from a hybrid amplifier and regenerator (HAR) device A (600) and a hybrid amplifier and regenerator (MAR) device B (610) converging on a hybrid amplifier and regenerator (HAR) device C (620). Each upstream transmission has a duration. Referring to FIGS. 7A and 7B, it is necessary that digital upstream traffic 650 tom the hybrid amplifier and regenerator (HAR) device A (600) and digital upstream traffic 660 from the hybrid amplifier and regenerator (HAR) device B (610) arrive at Me hybrid amplifier and regenerator (HAR) device C (620) at a certain time for correct operation. As mentioned earlier, the head end 144 sends the third type of downstream traffic on the downstream control and timing tone band 235 to correct the amplitude and/or phase (or timing) of the express band transmissions from any misaligned hybrid amplifier and regenerator (HAR) device 140.

In order to ensure the needed fine level of control, the express band carrier is an integral sub-multiple of the downstream control and timing tone (or carrier). In conjunction with the system head end 144 (as discussed earlier), the control units 500 from the hybrid amplifier and regenerator (HAR) device A (600) and the hybrid amplifier and regenerator (HAR) device B (610) send the digital upstream traffic 650 and the digital upstream traffic 660 at certain signal crossings of the downstream control and timing tone. Referring to FIG. 7B, the hybrid amplifier and regenerator (HAR) device A (600) finishes transmitting a symbol at a signal crossing 662 and the hybrid amplifier and regenerator (HAR) device B (610) must start sending the next symbol a short time later at a signal crossing 664 in order for the digital upstream traffic 650 and the digital upstream traffic 660 respectively to arrive at the hybrid amplifier and regenerator (HAR) device C (620) at the correct time (shown by a signal crossing 668) without overlaps or gaps or unintended carrier shifts. Digital upstream traffic 669 shows the digital upstream traffic 650 and the digital upstream traffic 660 combined or multiplexed correctly.

QAM modulation schemes are typically illustrated with a QAM constellation as shown in FIG. 7C. Since it is possible that multiple hybrid amplifier and regenerator (HAR) devices 140 will send upstream traffic to a single hybrid amplifier and regenerator (HAR) device 140, a null position 685 (i.e. no signal) is required in the QAM constellation to ensure that the upstream traffic from the multiple hybrid amplifier and regenerator (HAR) devices 140 can add in an analog fashion without creating constellation offsets in the express band receiver 450 in the upstream hybrid amplifier and regenerator (HAR) device 140. FIG. 7C shows a zero-zero data position (or an all zero position) shared with the null position 685. Alternatively, a dedicated null position (i.e. no signal) could be placed within the QAM constellation. It is important that the null position be input as part of the modulating signal in the express band transmitter 480 and not be formed by grounding out the output of the express band transmitter 480 during that time slot. This is to ensure that inter-symbol interference effects are treated linearly in the distributed express band transmitter 480 and add linearly into the express band receiver 450—which is designed on the assumption of linear inter symbol interference mitigation. If the null position is shared with the zero zero point, a long string of zeros in a virtual channel of the express band 260 is interpreted as no transmission, and packet preambles indicate the start of data with packet formatting indicating the end of data.

Before reliable upstream transmissions can take place in the cable (CATV) network 135, the Hybrid amplifier and regenerator (HAR) devices 140 and the second generation cable modems must be synchronized (or aligned). The synchronization is initially performed during power start-up of the cable (CATV) network 135. Since the second generation cable modems can be added at any time, the alignment and synchronization of the newly connected second generation cable modems can occur at any time.

The Hybrid amplifier and regenerator (HAR) devices 140 are synchronized first. Each digital regenerator 160 in the cable (CATV) network 135 has an unique hardware address and the system head end 144 knows the topology of the digital regenerators 160 in the system. All the regenerators 160 in each Hybrid amplifier and regenerator (HAR) device 140 initially turn off their express band transmitters 480 and listen for commands from the system head end 144 on the downstream control and timing tone band 235. The head end 144 sends a command addressed to the digital regenerator in first Hybrid amplifier and regenerator (HAR) device 140 downstream from the system head end 144 by modulating the downstream control and timing tone (typically using AM modulation as mentioned earlier). The command instructs the digital regenerator 160 to turn on its express band transmitter 480 and send an express band carrier with a specific phase and signal level. A receiver in the head end 144 detects the amplitude and phase of the express band carrier. If there is a significant difference between the desired amplitude and phase of the express band carrier and the actual amplitude and phase of the express band carrier received, the head end 144 sends a command on the downstream control and timing tone band 235 to the digital regenerator 160 to correct the amplitude and phase by the difference. The digital regenerator 160 corrects the phase of the express band carrier by adjusting the signal sent on the express band control line 505 to the express band transmitter 480 (i.e. the integer divider circuit in the control unit 500 now triggers the signal on an appropriate other phase crossing of the downstream control and timing tone). The digital regenerator 160 corrects the signal level by adjusting the signal sent on the express band control line 505 to the express band transmitter 480. (Alternatively, additional phase control can be achieved through an analog phase shifter for very fine control of phase for resolutions smaller than the inter-phase times of the downstream control and timing tone 235). If there is still a significant difference between the desired amplitude and phase of the 15 express band carrier and the actual amplitude and phase of the express band carrier received, the process iterates until the difference between the desired amplitude and phase of the

express band carrier and the actual amplitude and phase of the express band carrier received is insignificant.

Once the difference is insignificant, the system head end **144** turns to align the modulated data frame boundaries and symbol boundaries within each data frame of the express band Bitstream **264** from the digital regenerator **160**. The system head end **144** sends a command to the regenerator **160** instructing it to send a specific, repeated data sequence. E.g. all zeros in all virtual channels except for the designated virtual channel which carries all ones. The express band symbol rate is derived from the symbol rate of the traffic carried on the downstream control and timing tone. The symbol rates of the ramp band **250**, express band **260** and the downstream control and timing tone band **235** are integrally related (related by multiples of whole numbers). In this way, phase lock loops for the express band transmitter **450**, the ramp band receiver **460** and the clock for the time slot manager **470** can be synchronized amongst all the digital regenerators **160** by tracking the downstream control and timing band modulation rate. (Preferably, the modulation rate is also integrally related to the downstream control and timing tone or carrier). The system head end **144** receives the specified sequence sent from the digital regenerator **160** and examines it for the relative crossings of the sequence. Any offset from the desired timing (e.g. the crossing from zeros to ones at the maintenance channel boundary) is noted by the head end **144** which in turn sends adjustment commands to the digital regenerator **160**. The adjustment commands instruct the digital regenerator to shift the relative crossing of the symbols and repeated data frame by a specified number of phase crossings of the downstream control and timing tone or carrier. After the digital regenerator makes the requested adjustment, the multiplexing should be aligned. If not, other iterations of this process occurs. Since the downstream control and timing tone or carrier is normally many multiples of the modulation rate, vary fine control of each modulated data frame and the symbol boundaries within each data frame is possible.

Once the modulated data frame and symbol boundaries are aligned, the head end **144** sends a command to the digital regenerator **160** on the downstream control and timing tone **235** instructing the digital regenerator **160** to send zeros on all the virtual channels within the express band except the maintenance channel. The digital regenerator **160** (the "upstream digital regenerator") is also instructed by the head end **144** to take over part of the synchronization/alignment function for the digital regenerator **160** in the Hybrid amplifier and regenerator (HAR) device **140** immediately downstream of the upstream digital regenerator (the "downstream digital regenerator"). The head end **144** sends a command on the downstream control and timing tone band **235** to the downstream digital regenerator instructing the downstream digital regenerator **160** to transmit an express band carrier with a certain phase and amplitude. The upstream digital regenerator **160** reports the difference between the desired amplitude and phase of the express band carrier and the actual amplitude and phase of the express band carrier received by the upstream digital regenerator **160** to the system head end **144** in a message sent over the maintenance channel. If there is a significant difference between the desired amplitude and phase of the express band carrier and the actual amplitude and phase of the express band carrier received by the upstream digital regenerator **160**, the head end **144** sends a command on the downstream control and timing tone band **235** to the downstream digital regenerator **160** to correct the amplitude and phase by the difference. If there is still a significant difference between the desired amplitude and phase of the express band carrier and the actual amplitude and phase of the express band carrier received by the upstream digital regenerator **160**, the process iterates until the difference between the desired amplitude and phase of the express band carrier and the actual amplitude and phase of the express band carrier received by the upstream digital regenerator **160** is insignificant.

Once the amplitude and phase is aligned, the head end turns to align the modulated data frame and symbol boundaries. The head end **144** sends a command to the downstream digital regenerator **160** instructing it to send a specific, repeated data sequence. E.g. all zeros in all virtual channels except for a designated virtual channel which carries all ones. The upstream digital regenerator **160** receives the specified sequence sent from the downstream digital regenerator and examines it for the relative crossings of the sequence. Any offset from the desired timing (e.g. the crossing from zeros to ones at the channel boundary of the designated virtual channel) is noted by the upstream digital regenerator **160** which sends the offset to the system head end **144** in the maintenance channel. In response, the head end **144** sends adjustment commands to the digital regenerator **160**. The adjustment commands instruct the downstream digital regenerator **160** to shift the relative crossing of the symbols and repeated data frame by a specified number of phase crossings of the downstream control and timing tone or carrier. The downstream digital regenerator **160** corrects the misalignment of the express band data frame boundaries and the express band symbol boundaries by adjusting the signal sent on the time slot control line **505** to the time slot manager **470** (i.e. the integer divider circuit in the control unit **500** now triggers the signal sent on the time slot control line **505** on an appropriate other phase crossing of the downstream control and timing tone (or carrier)). After the digital regenerator makes the requested adjustment, the multiplexing should be aligned. If not, the process re-iterates.

If more than one downstream hybrid amplifier and regenerator (HAR) device **140** is connected to the upstream hybrid amplifier and regenerator (HAR) device **140**, the same process is applied to the other downstream hybrid amplifier and regenerator (HAR) device(s) **140** to align the amplitude, phase, the modulated, data frame and symbol boundaries.

The entire process repeats recursively for all the other digital regenerators in the Hybrid amplifier and regenerator (HAR) devices **140** in the cable (CATV) network **135**.

Once all the digital regenerators **160** are synchronized/aligned, the Hybrid amplifier and regenerator (HAR) devices **140** in the cable (CATV) network **135** are ready to receive ramp band traffic. The system head end **144** instructs all the Hybrid amplifier and regenerator (HAR) devices **140** to turn on their ramp band receivers **460** by sending a command in the downstream control and timing tone band **235**.

The second generation cable modems register onto the cable (CATV) network **135** using the same procedure used by the second generation cable modems in a cable (CATV) network **5** that does not have any digital regenerators **160** (or Hybrid amplifier and regenerator (HAR) devices **140**). That is, the second generation cable modems use the same procedure described in the DOCSIS specification.

When a second generation cable modem is first connected to the cable (CATV) network **135**, the second generation cable modem self tunes on the downstream cable modem band **232**. As mentioned earlier, the head end **144** periodi-

cally sends the time slot allocation map to all the second generation cable modems on the downstream cable modem band **232**. The recently connected second generation cable modem acquires the upstream time slot allocation map the next time the head end **144** sends it. The second generation cable modem examines the upstream time slot allocation map for explicitly labelled open (or contention) time slots. The recently connected second generation cable modem will randomly select one of the open time slots and attempt to use it by transmitting a registration request on the open time slot using its lowest signal level. Then the recently connected second generation cable modem waits to see whether a time slot is assigned to it by the head end **144** in the next time slot allocation map sent by the head end **144**. If a time slot is not assigned to the recently connected second generation cable modem in the upstream time slot allocation map, the recently connected second generation cable modem randomly selects another open time slot and transmits another registration request on the open time slot using the next highest signal level. This process will continue until the recently connected second generation cable modem sees the time slot it'selected assigned to it in the next upstream allocation map sent by the head end **144**.

At the ramp band receivers in each Hybrid amplifier and regenerator (HAR) device **140**, the following process occurs. The ramp band receiver **460** in the Hybrid amplifier and regenerator (HAR) device **140** immediately upstream from the recently connected second generation cable modem initially sees an idle line and examines it continuously for a valid packet preamble. All the second generation cable modems uses a specific packet preamble for upstream transmissions. If the recently connected second generation cable modem sends a registration request without a sufficient signal level, the ramp band receiver **460** will not receive a valid packet preamble. In addition, if the recently connected second generation cable modem sends a registration request at the same time that another recently connected second generation cable modem is transmitting, it is unlikely the ramp band receiver **460** will receive a valid registration request. Once the recently connected second generation cable modem sends a registration request with a sufficient signal level during an open time slot (i.e. no collisions with data from another second generation cable modem), the ramp band receiver **460** will receive a valid packet preamble and data containing the registration request. The Hybrid amplifier and regenerator (HAR) device **140** multiplexes the data containing the registration request into the designated virtual channel of the express band **260**. Once the system head end **144** receives the registration request in the designated virtual channel, the system head end **144** assigns the time slot used by the recently connected second generation cable modem to the recently connected second generation cable modem and sends another time slot allocation map to all the second generation cable modems. Furthermore, the system head end **144** will send a command to all the Hybrid amplifier and regenerator (HAR) devices **140** which use the same virtual channel to examine the signal level, the timing and frequency of the recently connected second generation cable modem during the time slot used by the recently connected second generation cable modem. The system head end **144** must send commands to all the HAR's **140** which use the same virtual channel because there is no way the system head end **144** knows from which HAR **140** received the original registration request from the recently connected second generation cable modem. (The system head end **144** only knows that a registration request has been mapped into a specific virtual channel which may be used by multiple HAR's **140**).

When the system head end **144** allocates an open time slot for any recently connected second generation cable modem to join the cable (CATV) network **135**, the system head end **144** does not know where the recently connected second generation cable modem **144**, if any, will be attached. Thus, during the free time slots (as specified in the time slot allocation map), all the HAR's **140** turn on their ramp band receivers **460** to detect initial transmission from any recently connected second generation cable modems. Alternatively, if during the open time slots, the HAR's **140** are set to note which ramp band receiver **460** (in the respective HAR **140**) is receiving a valid transmission and this is communicated to the system head end **144** over the maintenance channel (along with the identification of the respective HAR **140**), then the system head end **144** could limit the commands for fine tuning the cable modem transmissions to the ramp band receiver **460** in the respective HAR **140**. However, this alternative approach adds complexity.

If the ramp band receiver **460** of the Hybrid amplifier and regenerator (HAR) device **140** servicing the new second generation cable modem detects errors in the frequency, timing (i.e. time slot boundaries of the time slot), or signal level, the digital regenerator **160** reports the errors to the system head end **144** over the virtual maintenance channel. The system head end **144** sends adjustment commands to the recently connected second generation cable modem on the downstream cable modem transmission band **232** instructing the recently connected second generation cable modem to change its frequency, timing or signal level. Once the recently connected second generation cable modem is fine tuned, normal upstream transmission/traffic from the recently connected second generation cable modem to the head end **144** can proceed.

Other variations and modifications of the invention are possible. For example, different upstream traffic (e.g. telephony and Internet) can be carried simultaneously in different transmission formats within an analog band (e.g. QPSK, QAM, FSK, PSK, CDMA, etc). The ramp band **150** and the express band **260** will typically each handle a single transmission format. If all the upstream traffic is carried in a transmission format used by the ramp band **250**, then the reverse secondary analog amplifier **415** within each hybrid amplifier and regenerator (HAR) device is not required. (However, if a transmission format(s) for upstream traffic other than the transmission format used by the ramp band **250** is used, then the reverse secondary analog amplifier **415** in each hybrid amplifier and regenerator (HAR) device may be used to boost the upstream traffic (other than the ramp band and express band traffic).

Variations of the cable (CATV) network **135** are also possible. For example, the conventional trunk analog distribution amplifiers and analog distribution amplifiers can coexist in the same network with hybrid amplifier and regenerator (HAR) devices **140**, It is an engineering system design decision to determine the relative placement and spacing of these units. (For example, hybrid amplifier and regenerator (HAR) devices **140** may be placed on the trunk and the secondary trunks only and conventional analog distribution amplifiers may be placed on the feeder lines and the secondary feeder lines. Alternatively, hybrid amplifier and regenerator (HAR) devices, conventional trunk analog distribution amplifiers and conventional analog amplifiers can be placed in cyclic positions from the system head end **144** on the trunk **20**, secondary trunks **25**, feeder lines **30** and secondary feeder lines **35**)

Another variation of the cable (CATV) network **135** is possible. Referring in particular to FIG. **8**, the hybrid ampli-

fier and regenerator (HAR) devices are located only on the trunk **20** and the secondary trunks **25** (i.e. no hybrid amplifier and regenerator (HAR) devices **150** on the feeder lines **30** and the secondary feeder lines **35**). Conventional analog distribution amplifiers are used on the feeder lines **30** and the secondary feeder lines to boost the first, the second and third type of downstream traffic and the first, second and third type of upstream traffic. In particular, ramp band traffic in the ramp band **250** from the second generation cable modems are boosted by the conventional analog distribution amplifiers.

The upstream traffic is carried by the secondary feeder lines **35** and the feeder lines **30** to the hybrid amplifier and regenerator (HAR) devices at each junction where the feeder line **30** meets the trunk **20** or a secondary trunk **25**. Since the express band **260** is not used on the feeder lines **30**, the secondary feeder lines **35** and the subscriber lines **62**, an express band block filter **700** can be placed on each feeder line **30** near each junction where each feeder line **30** meets the trunk **20** or a secondary trunk **25**. The express band block filters prevent any signal or noise located in the express band **260** from entering the trunk **20** or any secondary trunk **25** from the feeder lines **30**. Since cable subscribers **60** are not typically connected to the trunk **20** or the secondary trunks **25**, noise in the express band **260** in the trunk **20** and the secondary trunks **25** is typically minimal. This reduction is noise improves the reliability and capacity of upstream traffic carried in the express band in the trunk **20** and the secondary trunks **25**. (It is also possible to physically place the express band block filter **700** inside each hybrid amplifier and regenerator (HAR) device near each junction where each feeder line **30** meets the trunk **20** or a secondary trunk **25**).

Furthermore, in the extreme, another variation to the cable (CATV) network **135** is possible. Referring in particular to FIG. **9**, an express band block filter **700** can be placed on every line **62** to each cable subscriber **60**. These express band block filters block or prevent any signal or noise in the express band **260** in the subscriber lines **62** from entering the feeder lines **30** or the secondary feeder lines **35**. Consequently, the ingress noise in the express band is typically substantially reduced in the trunk **20**, the secondary trunks **25**, the feeder lines **30** and the secondary feeder lines **35**. This reduction in noise improves the reliability and capacity of upstream traffic carried in the express band.

Yet another variation to the cable (CATV) network is possible. Referring in particular to FIGS. **10** and **11**, a first modified type of the hybrid amplifier and regenerator (HAR) device can be used in the feeder lines **30** and the secondary feeder lines **35**. As shown in FIG. **10**, the control unit **500** is modified so that the time slot manager **470** maps ramp band traffic **720** from a Hybrid amplifier and regenerator (HAR) device **140** into multiple virtual channels **730** in the express band Bitstream **740**. Ramp band traffic from different Hybrid amplifier and regenerator (HAR) devices **140** are mapped into different multiple virtual channels in the express band Bitstream **740**. This mapping (or multiplexing) technique provides redundancy and improved noise resilience in the cable (CATV) network. A second modified type of hybrid amplifier and regenerator (HAR) device is located near each junction where each feeder line **30** meets the trunk **20** or a secondary trunk **25**. Referring to FIG. **11**, the control unit **500** is modified so that the time slot manager **470** maps the multiple virtual channels **730** containing the ramp band traffic from the Hybrid amplifier and regenerator (HAR) device **140** into one virtual channel **745** in the express band Bitstream **748**. If possible, any discrepancies between the virtual channels are corrected by the second modified type of hybrid amplifier and regenerator (HAR) device. The remaining hybrid amplifier and regenerator (HAR) devices **140** on the trunk **20** and the secondary trunks **25** are not modified.

Another variation of the invention is possible. A plurality of ramp bands can be used. In this embodiment, ramp band traffic is the second type of upstream traffic carried in the ramp bands. All the ramp bands are separate from each other and are separate from the express band **260**. All the ramp bands and the express band **260** are in the reverse frequency band **240**. The ramp bands and the express band **260** are typically located below the first general upstream band **242** and above the second general upstream band **244**.

The ramp band traffic is carried in the cable (CATV) network **5** using digital signals modulated on a plurality of ramp band carriers using digital modulation techniques such as Quadrature Phase Shift Keying (QPSK) or Quadrature Amplitude Modulation (QAM). Each ramp band carrier is located in each ramp band respectively. The same modulation technique or different modulation techniques may be used on each ramp band. The speed of the ramp band traffic may be the same or different on each ramp band. (As mentioned earlier, the speed of the ramp band traffic typically will be between 320 Kbits/sec and 10 Mbits/sec).

A third modified type of hybrid amplifier and regenerator (HAR) device is used to map the upstream traffic in the ramp bands into the express band **260**. There are a plurality of ramp band receivers, one for each ramp band, in each third modified type of hybrid amplifier and regenerator (HAR) device. The ramp band receivers are designed to detect the digital signals carried on each of the ramp bands and convert them into a plurality of ramp band Bitstreams. Each ramp band Bitstream consists of a series of digital bits. For each ramp band, a fixed number of digital bits constitutes a ramp band symbol. Depending on the modulation scheme used for the respective ramp band traffic carried on each respective ramp band, the fixed number of digital bits constituting a ramp band symbol may be different or the same for the respective ramp band traffic carried on each respective ramp band. Each ramp band Bitstream contains the ramp band traffic carried on each ramp band respectively. (In particular, the ramp band receivers typically detect the phase and amplitude of the ramp band carriers carried in the ramp bands in order to detect and convert the digital signals carried in the respective ramp band traffic into the respective ramp band Bitstreams). A modified time slot manager and a modified control unit are used to map the each ramp band symbol in each ramp band Bitstream into the express band Bitstream. The modified control unit co-ordinates the digital time division multiplexing used to map the ramp band traffic from the ramp bands into the express band traffic carried in the express band **260**.

FIG. **12** shows three ramp bands **250**, **850** and **860** and one express band **260**. The ramp band **250** carries the ramp band traffic from the second generation cable modems. The ramp band **850** carries the ramp band traffic for Cornerstone Voice*, a product offered by Nortel*. Cornerstone Voice* uses special cable modems which provide telephony capability to cable subscribers. The ramp band **860** carries other ramp band traffic. As shown in FIG. **12**, the ramp band **250** and the ramp band **850** have the same bandwidth. The ramp band **860** has a smaller bandwidth than the ramp bands **250** and **860**. FIG. **12** also shows different modulation schemes for each ramp band (shown by the different hatching).

Referring to FIG. **13**, the third modified type of hybrid amplifier and regenerator (HAR) device is used to map the

upstream traffic in ramp bands **250**, **850** and **860** into the express band **260**. In addition to the ramp band receiver **460**, the digital regenerator **464** in the third modified type of hybrid amplifier and regenerator (HAR) device utilizes two additional ramp band receivers **950**, **960**. The ramp band receivers **460**, **950** and **960** are designed to detect and convert the digital signals carried the ramp bands **250**, **850** and **860** respectively into three ramp band Bitstreams. (In particular, the ramp band receivers **460**, **950** and **960** detect the phase and amplitude of the ramp band carriers carried in the ramp bands **250**, **850** and **860** respectively). A modified time slot manager *Trade-maark is used to map the each ramp band symbol in each ramp band Bitstream into the express band. A modified control unit coordinates the digital time division multiplexing used to map the upstream traffic from the ramp bands into the express band Bitstream.

Another variation of the invention is possible. The upstream traffic in one ramp band can be mapped into a plurality of express bands using digital time division multiplexing. In this embodiment, express band traffic is the second type of upstream traffic carried in the express bands. All the express bands are separate from each other and are separate from the ramp band **250**. All the express bands and the ramp band **250** are in the reverse frequency band **240**. The express bands and the ramp band **250** are typically located below the first general upstream band **242** and above the second general upstream band **244**.

The express band traffic is carried in the cable (CATV) network **135** using digital signals modulated on a plurality of express band carriers using known modulation techniques such as 16 or 64 Quadrature Amplitude Modulation (QAM). Each express band carrier is located in each express band respectively. The same modulation technique or different modulation techniques may be used on each express band. The speed of the express band traffic may be the same or different on each express band. It is normally the same. (As mentioned earlier, the speed of the express band traffic typically will be between 20 Mbits/sec and 40 Mbits/sec).

A fourth modified type of hybrid amplifier and regenerator (HAR) device is used to map the upstream traffic in the ramp band **250** into the express bands. There are a plurality of express band receivers, one for each express band, in each fourth modified type of hybrid amplifier and regenerator (HAR) device. All the express band receivers are designed to detect and convert the digital signals carried in each respective express band into a plurality of express band Bitstreams. Each express band Bitstream consists of a series of digital bits. A second modified time slot manager and a second modified control unit are used to map the each ramp band symbol in the ramp band Bitstream typically into one of the express band Bitstreams. The second modified control unit coordinates the digital time division multiplexing used to map the ramp band traffic from the ramp band into the express band Bitstreams. (For example, a plurality of fourth modified type of hybrid amplifier and regenerator (HAR) devices in one part of the cable (CATV) network can map the ramp band traffic into a certain express band. Another plurality of fourth modified type of hybrid amplifier and regenerator (HAR) devices in another part of the cable (CATV) network can map the ramp band traffic into another express band, etc). The second modified time slot manager could also map each ramp band symbol in the ramp band Bitstream into a plurality of the express band Bitstreams or all of the express band Bitstreams for redundancy and improved resilience.

Yet another variation of the invention is possible. The ramp band traffic in a plurality of ramp bands can be mapped into a plurality of express bands using digital time division multiplexing. This variation is suitable for cable (CATV) networks that have heterogeneous cable modems which have non-interchangeable related modulation rates. In this embodiment, the express band traffic is the second type of upstream traffic carried in the express bands. All the express bands are separate from each other and are separate from the ramp bands **250**. All the express bands and the ramp band **250** are in the reverse frequency band **240**. The express bands and the ramp bands **250** are typically located below the first general upstream band **242** and above the second general upstream band **244**.

The express band traffic is carried in the cable (CATV) network **135** using digital signals modulated on a plurality of express band carriers using known modulation techniques such as 16 or 64 Quadrature Amplitude Modulation (QAM). Each express band carrier is located in each express band respectively. The same modulation technique or different modulation techniques may be used on each express band. The speed of the express band traffic may be the same or different on each express band. It is normally the same. (As mentioned earlier, the speed of the express band traffic, typically will be between 20 Mbits/sec and 40 Mbits/sec). This embodiment requires multiple downstream control and timing tones (one for each express band).

Certain Hybrid amplifier and regenerator (HAR) devices **140** map the ramp band traffic in one of the ramp bands to one of the express bands. Other Hybrid amplifier and regenerator (HAR) devices **140** map the ramp band traffic in another ramp band to another express band, etc.

All such modifications or variations are believed to be within the sphere and scope of the invention as defined by the claims appended hereto.

We claim:

1. A hybrid amplifier and regenerator (HAR) device for use in a communications network for carrying downstream traffic in a forward frequency band and for carrying digital upstream traffic in a reverse frequency band spaced from the forward frequency band and below the forward frequency band, the hybrid amplifier and regenerator (HAR) device comprising:

an analog amplifier for amplifying said downstream traffic; and

a digital regenerator, wherein said digital regenerator comprises:

mapping circuitry for mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express band which is also part of the reverse frequency band but spaced from the at least one ramp band, wherein the at least one express band transports upstream traffic at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from the at least one ramp band into the at least one express band; and

an express band transmitter for transmitting digital upstream traffic from the mapping circuitry in the at least one express band.

2. A hybrid amplifier and regenerator (HAR) device according to claim **1**, wherein said mapping circuitry uses digital time division multiplexing to map the digital upstream traffic carried in said at least one ramp band to the digital upstream traffic carried in said at least one express band.

3. A hybrid amplifier and regenerator (HAR) device according to claim 2, wherein there are a plurality of ramp bands and only one express band.

4. A hybrid amplifier and regenerator (HAR) device according to claim 2, wherein there are a plurality of express bands and only one ramp band.

5. A hybrid amplifier and regenerator (HAR) device according to claim 2, wherein there are only one ramp band and one express band.

6. A hybrid amplifier and regenerator (HAR) device according to claim 5, wherein said mapping circuitry comprises:

a diplex filter to separate the digital upstream traffic carried in the ramp band from the digital upstream traffic carried in the express band;

a ramp band receiver to detect the digital upstream traffic carried in the ramp band, said ramp band receiver being connected to the diplex filter;

an express band receiver to detect the digital upstream traffic carried in the express band, said express band receiver being connected to the diplex filter;

a time slot manager for mapping the digital upstream traffic carried in the ramp band from the ramp band receiver to the digital upstream traffic carried in the express band from the express band receiver, said time slot manager being connected to the ramp band receiver and the express band receiver; and

a control unit for controlling the mapping of the digital upstream traffic carried in the ramp band to the digital upstream traffic carried in the express band, said control unit being connected to the time slot manager, the ramp band receiver and the express band receiver.

7. A hybrid amplifier and regenerator (HAR) device according to claim 1 further comprising a reverse secondary analog amplifier for amplifying upstream traffic carried in at least one general upstream band which is part of the reverse frequency band but spaced from the at least one ramp band and the at least one express band.

8. A hybrid amplifier and regenerator (HAR) device according to claim 7, wherein the reverse secondary analog amplifier comprises:

a diplex or a triplex filter to separate the upstream traffic carried in the at least one general band from the upstream traffic carried in the at least one ramp band and the at least one express band; and

an analog amplifier for amplifying the upstream traffic carried in at least one general upstream band.

9. A hybrid amplifier and regenerator (HAR) according to claim 7, wherein said at least one general frequency band comprises a first general frequency band and a second general frequency band.

10. A digital regenerator for use in hybrid amplifier and regenerator (HAR) device, the digital regenerator comprising:

mapping circuitry for mapping digital upstream traffic carried in at least one ramp band which is part of a reverse band to digital upstream traffic carried in at least one express band which is also part of the reverse band but spaced from the at least one ramp band, wherein the at least one express band transports upstream traffic data at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from the at least one ramp band into the at least one express band; and

an express band transmitter for transmitting digital upstream traffic from the mapping circuitry in said at least one express band.

11. A digital regenerator according to claim 10, wherein said mapping circuitry uses digital time division multiplexing to map the digital upstream traffic carried in said at least one ramp band to the digital upstream traffic carried in said at least one express band.

12. A digital regenerator according to claim 11, wherein there are a plurality of ramp bands and only one express band.

13. A digital regenerator according to claim 11, wherein there are a plurality of express bands and only one ramp band.

14. A digital regenerator according to claim 11, wherein there are only one ramp band and one express band.

15. A digital regenerator according to claim 14, wherein said mapping circuitry comprises:

a diplex filter to separate the digital upstream traffic carried in the ramp band from the digital upstream traffic carried in the express band;

a ramp band receiver to detect the digital upstream traffic carried in the ramp band, said ramp band receiver being connected to the diplex filter;

an express band receiver to detect the digital upstream traffic carried in the express band, said express band receiver being connected to the diplex filter;

a time slot manager for mapping the digital upstream traffic carried in the ramp band from the ramp band receiver to the digital upstream traffic carried in the express band from the express band receiver, said time slot manager being connected to the ramp band receiver and the express band receiver; and

a control unit for controlling the mapping of the digital upstream traffic carried in the ramp band to the digital upstream traffic carried in the express band, said control unit being connected to the time slot manager, the ramp band receiver and the express band receiver.

16. A communications network for carrying downstream traffic from a system head end to a plurality of cable subscribers within a forward frequency band, and for carrying digital upstream traffic from the plurality of cable subscribers to the system head end in a reverse frequency band which is spaced from the forward frequency band and below the forward frequency band, the communications network comprising:

(a) transmission means for interconnecting the system head end and the plurality of cable subscribers;

(b) a plurality of hybrid amplifier and regenerator (HAR) devices located at spaced intervals along the transmission means, each hybrid amplifier and regenerator (HAR) device comprising:

amplification circuitry for amplifying said downstream traffic; and

a digital regenerator, wherein said digital regenerator comprises:

mapping circuitry for mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express band which is also part of the reverse frequency band but spaced from the at least one ramp band, wherein the at least one express band transports upstream traffic data at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from the at least one ramp band into the at least one express band; and

an express band transmitter for transmitting digital upstream traffic from the mapping circuitry in said at least one express band; and

(c) cable modems for receiving the downstream traffic for the cable subscribers and for sending the digital upstream traffic from the cable subscribers in said at least one ramp band.

17. A communications network according to claim 16, wherein the transmission means comprise a trunk, a plurality of secondary trunks, a plurality of feeder lines, a plurality of secondary feeder lines and a plurality of subscriber lines.

18. A communication network according to 17, wherein the trunk and the secondary trunks use fibre optic cable, the feeder lines, the secondary feeder lines and the subscriber lines use coaxial cable and the transmission means further comprise a plurality of fibre nodes used to interconnect the coaxial cable with the fibre optic cable.

19. A communications network according to claim 17, wherein the transmission means use coaxial cable.

20. A communications network according to claim 17 further comprising a plurality of express band block filters, each express band block filter being placed on each feeder line near the trunk or near one of the secondary trunks.

21. A communications network according to claim 17 further comprising a plurality of express band block filters, each express band block filter being placed on each subscriber line.

22. A communications network according to claim 17 further comprising a plurality of trunk analog distribution amplifiers located at spaced intervals along the trunk and the secondary trunks and a plurality of analog distribution amplifiers located at spaced intervals along the feeder lines and the secondary feeder lines and wherein the trunk analog distribution amplifiers and the analog distribution amplifiers amplify the downstream traffic and the upstream traffic.

23. A method for carrying in a communications network downstream traffic in a forward frequency band and digital upstream traffic in a reverse frequency band which is spaced from the forward frequency band and below the forward frequency band, the method comprising:

amplifying and transmitting said downstream traffic in the forward frequency band;

mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express bands which is also part of the reverse frequency band but spaced from the at least one ramp band, wherein the at least one express band transports upstream traffic data at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from the at least one ramp band into the at least one express band; and

transmitting digital upstream traffic in the at least one express band.

24. A method according to claim 23, wherein the mapping uses digital time division multiplexing.

25. A method according to claim 24, wherein there are a plurality of ramp bands and only one express band.

26. A method according to claim 24, wherein there are a plurality of express bands and only one ramp band.

27. A method according to claim 24, wherein there are only one ramp band and one express band.

28. A method for processing digital upstream traffic in a digital regenerator, the method comprising:

mapping digital upstream traffic carried in at least one ramp band which is part of the reverse frequency band to digital upstream traffic carried in at least one express band which is also part of the reverse frequency band but spaced from the at least one ramp band, wherein the at least one express band transports upstream traffic data at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from the at least one ramp band into the at least one express band; and

transmitting digital upstream traffic in the at least one express band.

29. A method according to claim 28, wherein said mapping uses digital time division multiplexing.

30. A method according to claim 29, wherein there are a plurality of ramp bands and only one express band.

31. A method according to claim 29, wherein there are a plurality of express bands and only one ramp band.

32. A method according to claim 29, wherein there are only one ramp band and one express band.

33. A hybrid amplifier and regenerator (HAR) device for use in a communications network for carrying downstream traffic in a forward frequency band and for carrying digital upstream traffic in a reverse frequency band spaced from the forward frequency band and below the forward frequency band, the hybrid amplifier and regenerator (EAR) device comprising:

an analog amplifier for amplifying said downstream traffic; and

a digital regenerator, wherein said digital regenerator comprises:

mapping circuitry for mapping digital upstream traffic carried in a ramp band which is part of the reverse frequency band to a plurality of virtual channels carried in an express band which is also part of the reverse frequency band but spaced from the ramp band, wherein the at least one express band transports upstream traffic data at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from tie at least one ramp band into the at least one express band; and

an express band transmitter for transmitting the virtual channels from the mapping circuitry in the express band.

34. A hybrid amplifier and regenerator (HAR) device for use in a communications network for carrying downstream traffic in a forward frequency band and For carrying digital upstream traffic in a reverse frequency band spaced from the forward frequency band and below the forward frequency band, the hybrid amplifier and regenerator (HAR) device comprising:

an analog amplifier for amplifying said downstream traffic, and

a digital regenerator, wherein said digital regenerator comprises:

mapping circuitry for mapping digital upstream traffic carried in a plurality of virtual channels in an express band which is part of the reverse frequency band to a single virtual channel in the express band, wherein the at least one express band transports upstream traffic data at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from the at least one ramp band into the at least one express band; and

an express band transmitter for transmitting the single virtual channel from the mapping circuitry in the express band.

35. A digital regenerator for use in a hybrid amplifier and regenerator (HAR) device, the digital regenerator comprising:

mapping circuitry for mapping digital upstream traffic carried in a ramp band which is part of a reverse frequency band to a plurality of virtual channels carried in an express band which is also part of the reverse frequency band but spaced from the ramp band, wherein the at least one express band transports upstream traffic data at a substantially higher data rate as compared to the at least one ramp band so that upstream traffic originating from a plurality of sources can be aggregated from the at least one ramp band into the at least one express band; and

an express band transmitter for transmitting the virtual channels from the mapping circuitry in the express band.

36. A digital regenerator for use in a hybrid amplifier and regenerator (HAR) device the digital regenerator comprising:

mapping circuitry for mapping digital upstream traffic carried in a plurality of virtual channels in an express band which is part of a reverse frequency band to a single virtual channel in the express band, wherein the single virtual channel transports upstream traffic data at a substantially higher data rate as compared to any one of the plurality of virtual channels so that upstream traffic originating from a plurality of sources can be aggregated from the plurality of virtual channels into the single virtual channel; and

an express band transmitter for transmitting the single virtual channel from the mapping circuitry in the express band.

37. A method for multiplexing a plurality of express band transmissions, each express band transmission having a duration, from a plurality of respective downstream hybrid amplifier and regenerator (HAR) devices at an upstream hybrid amplifier and regenerator (HAR) device in a communications network, the method comprising:

a) determining a start time for each express band transmission which ensures that the express band transmissions will arrive at the upstream hybrid amplifier and regenerator (HAR) device without interfering with each other, and,

b) beginning each express band transmission from each respective downstream hybrid amplifier and regenerator (HAR) device at each respective start time;

wherein the transmitting step uses a Quadrature Amplitude Modulation (QAM) scheme represented by a QAM constellation having a null position.

38. A method according to claim 37, wherein the QAM constellation has an all zero position and the all zero position is shared with the null position.

39. A method for multiplexing a plurality of express band transmissions, each express band transmission having a duration and being modulated on an express band carrier within an express band, from a plurality of respective downstream hybrid amplifier and regenerator (HAR) devices at an upstream hybrid amplifier and regenerator (HAR) device in a communications network having a head end, the method comprising:

a) transmitting from the head end a downstream control and timing tone in an downstream control and timing tone band which is separate and apart from the express band wherein the express band carrier is an integral sub-multiple of the downstream control and timing tone.

b) determining a signal crossing of the downstream control and timing tone for each express band transmission upon which each respective express band transmission will begin which ensures that the express band transmissions will arrive at the upstream hybrid amplifier and regenerator (HAR) device without interfering with each other; and,

c) beginning each express band transmission from each respective downstream hybrid amplifier and regenerator (HAR) device at each respective signal crossing.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

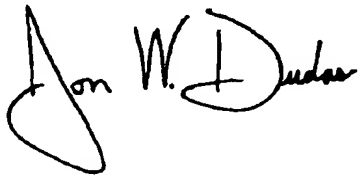
PATENT NO. : 6,598,232 B1
DATED : July 22, 2003
INVENTOR(S) : James A. McAlear

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 32,
Line 28, the word "hand" should be -- band --.
Line 29, the word "hand" should be -- band --.
Line 43, the word "For" should be -- for --.

Signed and Sealed this

Fifteenth Day of June, 2004



JON W. DUDAS
Acting Director of the United States Patent and Trademark Office

US006157812A

United States Patent [19]

Sarraf

[11] Patent Number: 6,157,812

[45] Date of Patent: Dec. 5, 2000

[54] **SYSTEM AND METHOD FOR ENHANCED SATELLITE PAYLOAD POWER UTILIZATION**

[75] Inventor: **Jamal Sarraf**, Irvine, Calif.

[73] Assignee: **Hughes Electronics Corporation**, El Segundo, Calif.

[21] Appl. No.: **08/944,879**

[22] Filed: **Oct. 6, 1997**

[51] **Int. Cl.**[7] **H04B 7/185**

[52] **U.S. Cl.** **455/13.4**; 455/13.3; 370/318; 370/316

[58] **Field of Search** 455/13.3, 13.4, 455/12.1, 427, 428, 429, 430; 342/353, 352; 370/316, 326, 318, 311

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,009,345	2/1977	Flemming et al.	179/15
5,550,550	8/1996	Das	342/353
5,818,385	10/1998	Bartholomew	342/372
5,832,379	11/1998	Mallinckrodt	455/427
5,878,329	3/1999	Mallinckrodt	455/69
5,940,753	8/1999	Mallinckrodt	455/422

FOREIGN PATENT DOCUMENTS

0762637 A2	8/1996	European Pat. Off. .
63-185129A	1/1987	Japan .

Primary Examiner—Fan Tsang

Attorney, Agent, or Firm—Bradley K. Lortz; Vihayalakshmi D. Duraiswamy; Michael W. Sales

[57] **ABSTRACT**

Systems and methods for improved use of idle power of each satellite repeater/transponder during low-traffic periods improve the overall link performance in multi-carrier, demand-assigned satellite communication systems through dynamic control and allocation of additional power to all signal carriers passing through each repeater when the total traffic load in the repeater is below a threshold. For satellite systems already in operation, the invention can be implemented and integrated into the existing feeder earth stations. For new systems, the invention can be implemented and integrated into the transmit section of individual satellite repeaters/transponders. The invention can be applied to new satellite systems to directly reduce the required satellite payload power for a given mission, thus substantially lowering the cost of the space segment. For existing systems, the benefits may be applied toward increasing the total number of carriers supported by the system, increasing the average quality and availability for the downlinks, increasing the system coverage and service area, or any combination thereof.

11 Claims, 4 Drawing Sheets

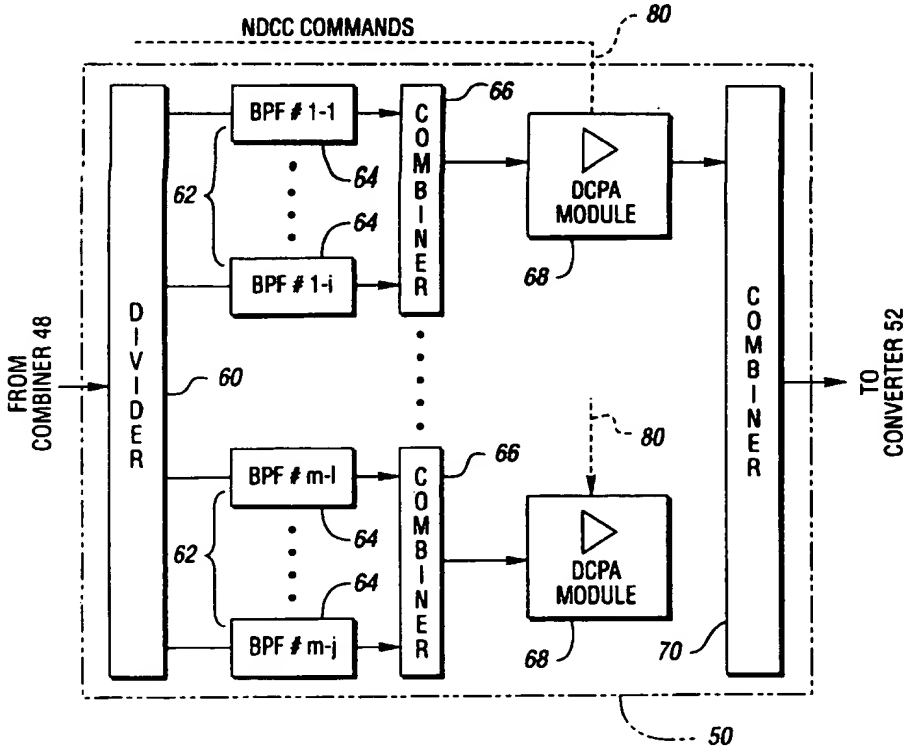
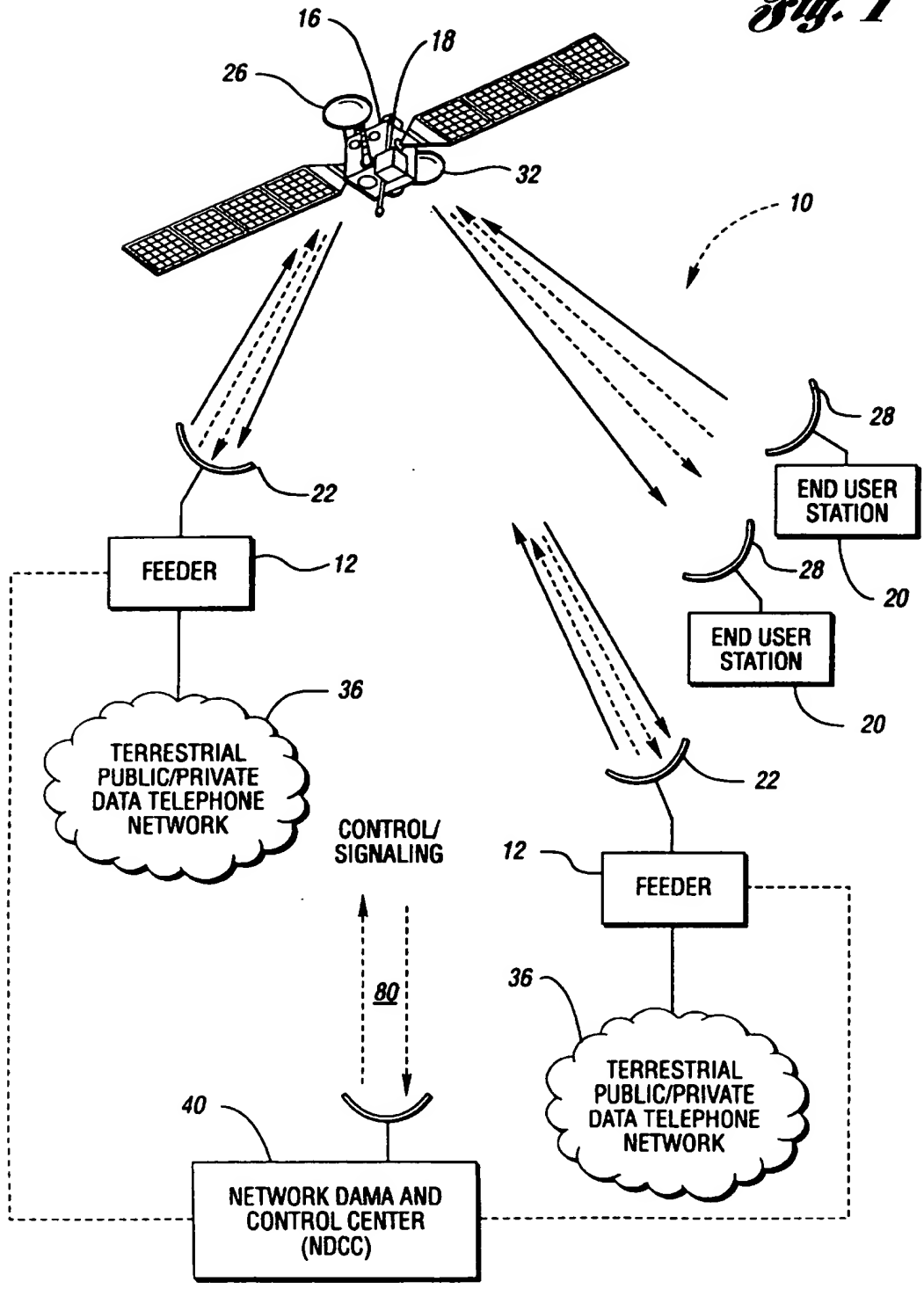


Fig. 1


16
18
26
32
10
28
END USER STATION
20
28
END USER STATION
20
22
22
FEEDER
12
12
FEEDER
36
TERRESTRIAL PUBLIC/PRIVATE DATA TELEPHONE NETWORK
CONTROL/ SIGNALING
80
36
TERRESTRIAL PUBLIC/PRIVATE DATA TELEPHONE NETWORK
40
NETWORK DAMA AND CONTROL CENTER (NDCC)

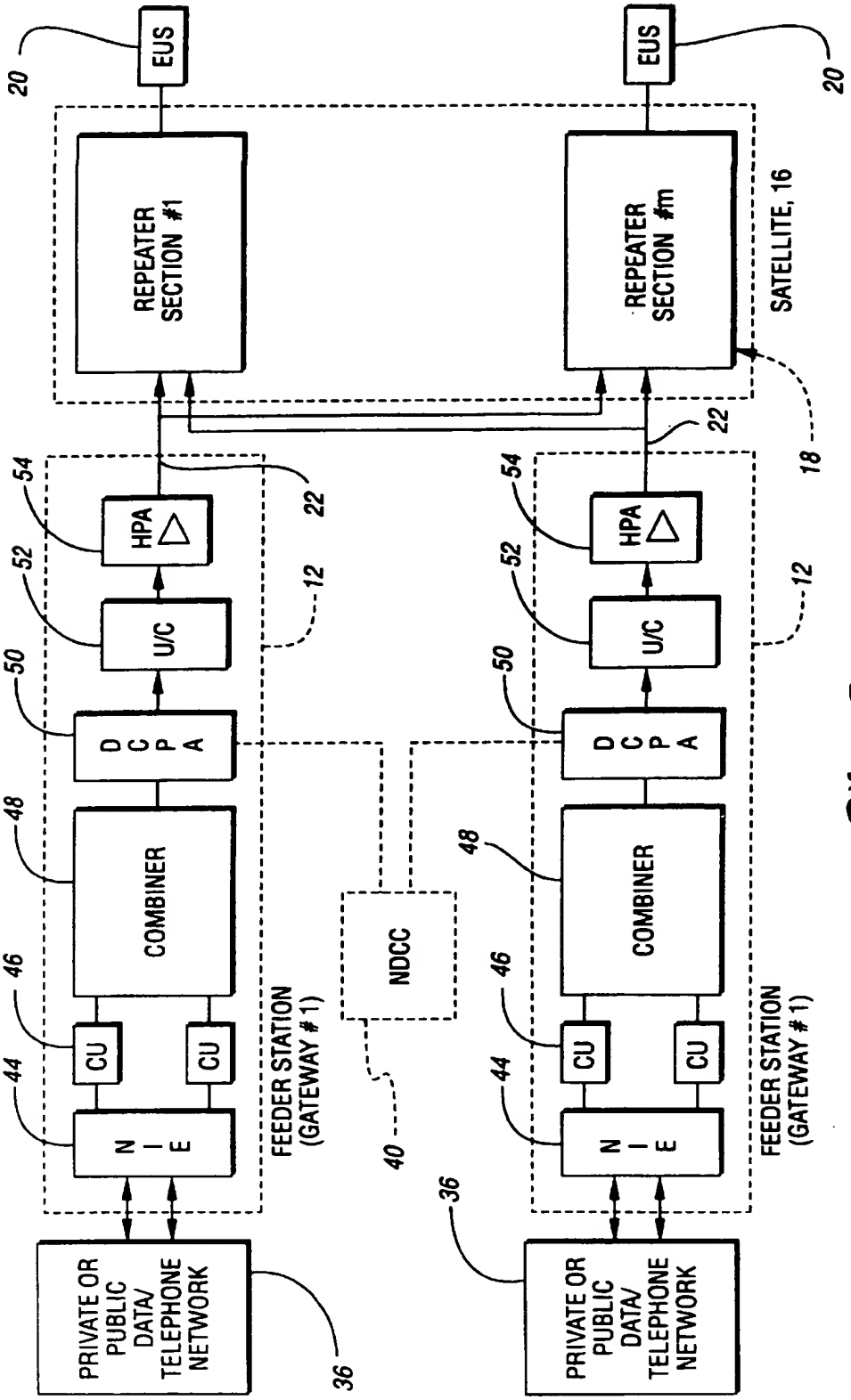

EUS
20
REPEATER SECTION #1
REPEATER SECTION #m
SATELLITE, 16
18
22
HPA
54
U/C
52
DCPA
50
COMBINER
48
CU
46
NIE
44
NDCC
40
FEEDER STATION (GATEWAY # 1)
12
PRIVATE OR PUBLIC DATA/ TELEPHONE NETWORK
36

Fig. 2

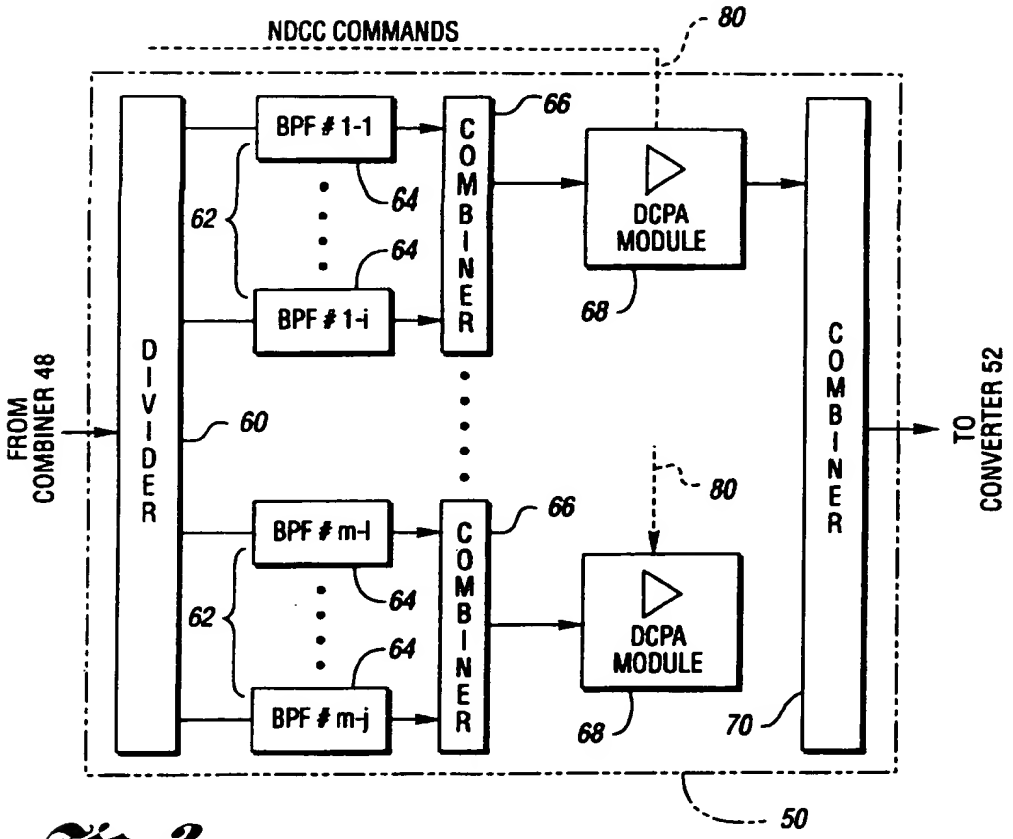
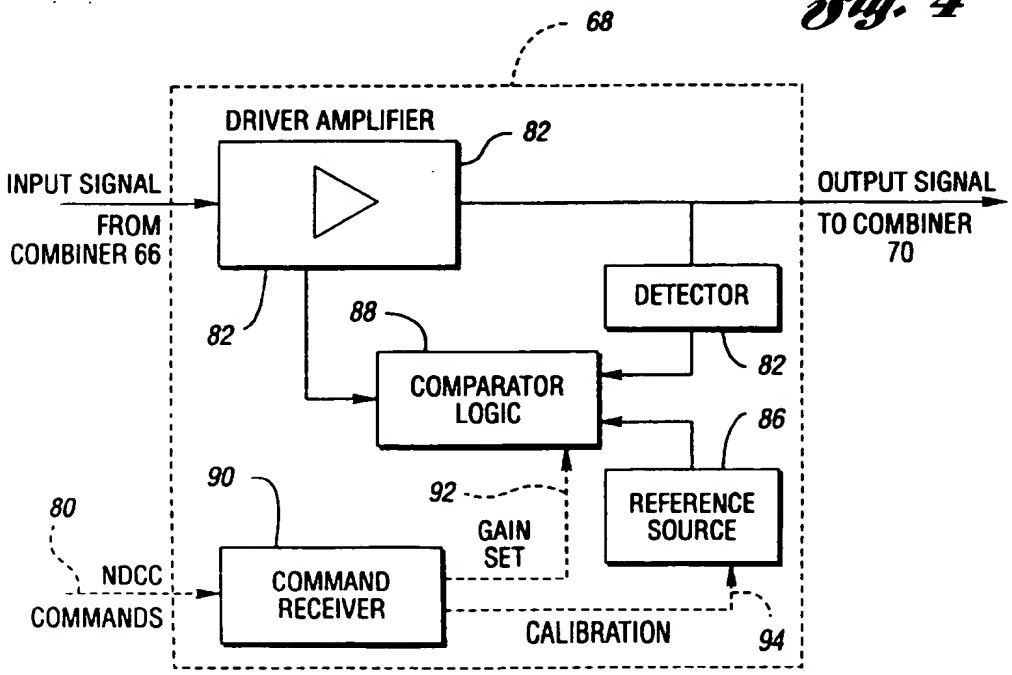

NDCC COMMANDS
80
FROM COMBINER 48
DIVIDER
60
62
BPF # 1-1
64
BPF # 1-i
64
COMBINER
66
DCPA MODULE
68
BPF # m-l
64
BPF # m-j
64
COMBINER
66
DCPA MODULE
68
80
COMBINER
70
TO CONVERTER 52
50

Fig. 3

Fig. 4


68
DRIVER AMPLIFIER
82
INPUT SIGNAL
FROM COMBINER 66
OUTPUT SIGNAL
TO COMBINER 70
DETECTOR
82
88
COMPARATOR LOGIC
86
REFERENCE SOURCE
90
92
GAIN SET
80
NDCC COMMANDS
COMMAND RECEIVER
CALIBRATION
94

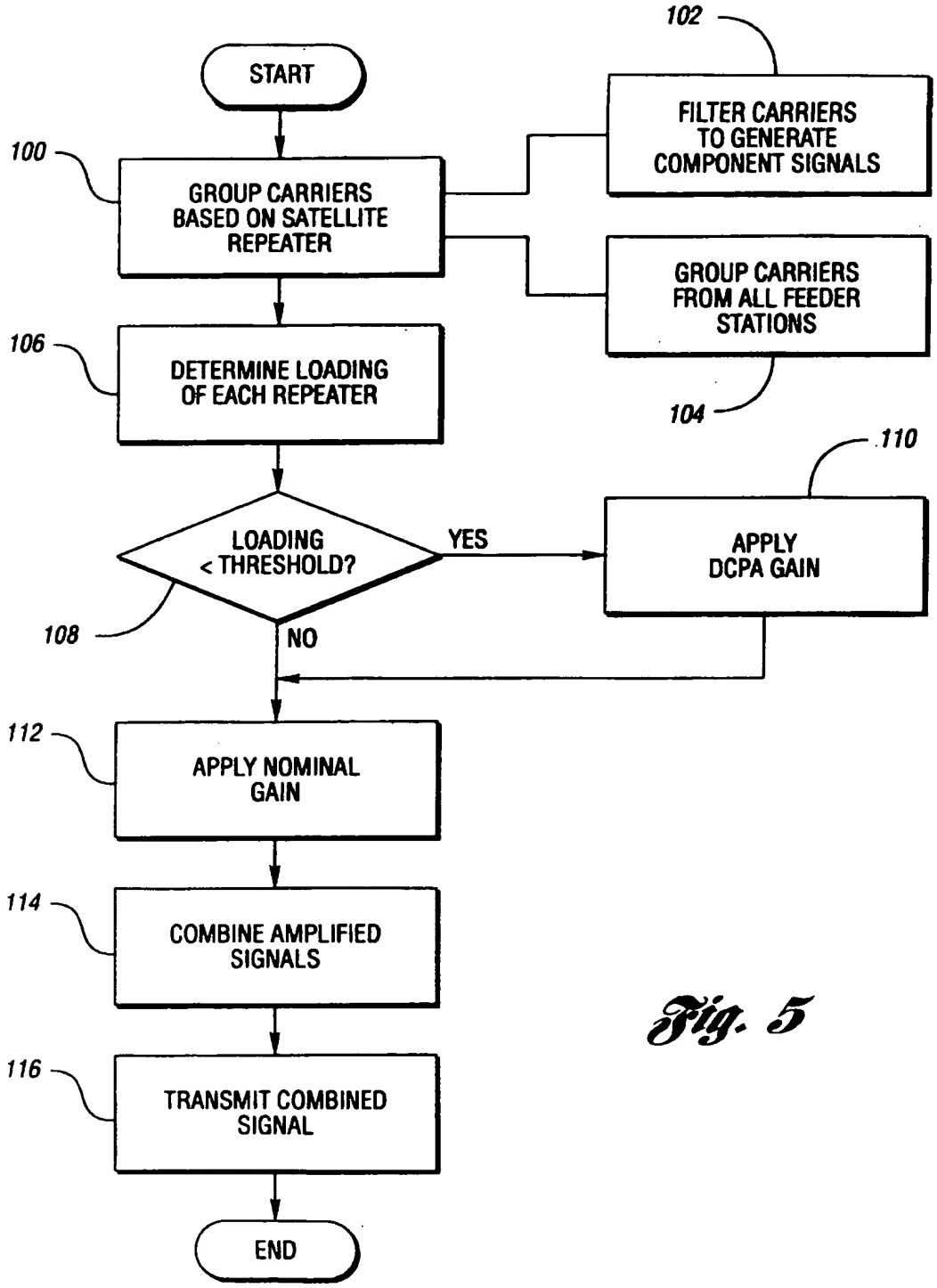

START
100
GROUP CARRIERS BASED ON SATELLITE REPEATER
102
FILTER CARRIERS TO GENERATE COMPONENT SIGNALS
GROUP CARRIERS FROM ALL FEEDER STATIONS
104
106
DETERMINE LOADING OF EACH REPEATER
LOADING < THRESHOLD?
YES
108
NO
110
APPLY DCPA GAIN
112
APPLY NOMINAL GAIN
114
COMBINE AMPLIFIED SIGNALS
116
TRANSMIT COMBINED SIGNAL
END

Fig. 5

SYSTEM AND METHOD FOR ENHANCED SATELLITE PAYLOAD POWER UTILIZATION

TECHNICAL FIELD

The present invention relates generally to communication systems, and more particularly, to satellite communication systems.

BACKGROUND ART

Satellite communication systems are widely used to support video, voice and data communication services all over the world. In recent years such services are being delivered to the individual end-user directly via small fixed or mobile terminals on a point-to-point basis.

Handheld mobile terminals, and other ultra-small aperture personal terminals are expected to be widely used with all types of satellite systems for mobile and fixed telephony, data/fax, interactive bandwidth-on-demand, and multimedia applications.

All such satellite systems rely on the use of any one or a combination of single channel per carrier (SCPC), time-division multiple-access (TDMA) or code-division multiple-access (CDMA) transmission technologies. Such systems result in transmission of a large number of signal carriers in a frequency-division multiple-access (FDMA) arrangement, and on a demand-assigned multiple-access (DAMA) basis. In these systems each user is allowed to access and use the system only when the user has a need, and even then the system resources are assigned to the user based on demand. From the perspective of a satellite communication system, users do not have a dedicated full-time transmission channel but rather share such channels with other users. Moreover, signal transmissions from end-user terminals to the satellite do not need to occur unless there is information to be transmitted.

Examples of such satellite communication systems include geosynchronous (GSO) and non-geosynchronous (NGSO) earth orbit systems which are being deployed for mobile and fixed telephony applications, in addition to the new wide-band systems for bandwidth-on-demand and point-to-point multimedia services. To meet the business requirements for high-capacity and wide-area coverage capabilities, most such systems employ a large number of very high-gain spot beams.

In general, communications satellites can cover a large geographical area via a single or several communications beams (reaching even a few hundred beams in some cases). The total available radio frequency spectrum for each satellite beam is generally broken up into a number of smaller channels. Each radio frequency channel can be used, based on many system design objectives, to carry signals using any of the three transmission technologies (SCPC, TDMA, or CDMA) noted above. In demand-assigned systems, transmission of the signal carrier by each user terminal in any channel is managed by a central system controller. The power level of each carrier, and how much of the satellite downlink power is used by that carrier, is determined by many system parameters but is generally fixed once it is determined. However, such systems typically employ uplink power control to compensate for propagation anomalies so that the signal level received at the satellite is relatively constant.

On board the satellite, each downlink beam carries signals from one or more payload repeaters. Repeaters may be of the bent-pipe (transponder) or regenerative types, using analog or digital signal processing technologies. Each repeater may have a dedicated high-power amplifier (HPA) or share a hybrid-matrix amplifier assembly with other repeaters. Each repeater may also be assigned to a single signal carrier or be used to support several carriers. All such high-power amplifier assemblies supporting multiple carriers are operated in a linear mode.

The total downlink power of each satellite is divided among its repeaters based on the projected traffic capacity of each repeater. With bent-pipe designs, the repeater power is also pre-allocated to each carrier based on a maximum number of such carriers the repeater must support. In other words, a predetermined portion of the repeater power is always reserved for each signal carrier whether or not that carrier is actually present. With regenerative designs, where user traffic through each repeater is generally multiplexed into a single downlink time-division multiplexed (TDM) carrier, the repeater power is fully utilized at all times regardless of traffic volume. This guarantees the availability of power to each carrier (or user data burst) during heavy traffic periods when each repeater is expected to be loaded at its maximum capacity. However, as with all demand-assigned multiple-access transmission techniques, the peak system loading occurs only during a small fraction of the daily or periodic operations. Moreover, the peak traffic loading for each repeater usually occurs a few years after the system start when the full population of user terminals are deployed and operational.

As such, satellite based communication systems are deployed with a capacity to support a system which generally reaches its maximum traffic loading several years later. Even then, the full payload power of each repeater is utilized only for a small fraction of the time during the peak daily traffic hours. For all other times, the power of each repeater is reserved for many channels or carriers which are not active. Recognition of this gross under-utilization of the expensive satellite payload power provides significant opportunity for improvement as accomplished by the present invention.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a system and method for more efficient utilization of the power for each satellite repeater/transponder during low-traffic periods to improve the overall performance of the system in a multi-carrier, demand-assigned satellite communication system. In such systems, the satellite payload is generally made up of a number of non-regenerative (bent-pipe), repeater sections where each repeater processes the active signal carriers present within a particular portion of the satellite frequency spectrum. Such repeaters operate in a linear mode where the amount of downlink power of each signal carrier (as received at the satellite) is directly proportional to the level transmitted by a ground station. Such systems may also employ uplink power control to compensate for various propagation anomalies and maintain a relatively constant signal level.

It is a further object of the present invention to provide systems and methods for enhancing the utilization of satellite power, dynamically and automatically, by allocating the power of each repeater among the signal carriers passing through it in accordance with current traffic loading conditions. As such, during low-traffic periods each carrier receives a certain additional amount of downlink power (compared to the lower full-load value) resulting in a substantial improvement in system performance.

The present invention can be implemented as either a ground-based system or a satellite-based system. For existing satellite systems (already launched and operational), the present invention can be integrated into the existing ground equipment infrastructure. For new systems, the present invention is preferably implemented as part of the satellite payload itself.

In carrying out the above objects and other objects and features of the present invention for a ground-based implementation, a system for controlling the power level of uplink carriers is provided to improve the utilization of satellite repeater power. The system is implemented as a dynamic carrier power allocation (DCPA) assembly at each feeder earth station or alternatively integrated with the satellite payload of a communication network. The DCPA assembly includes DCPA-driver amplifier modules and associated circuitry which is inserted before the upconverter and high-power amplifier (HPA) assembly within the ground station. At each feeder station the DCPA assembly collects and groups all the out-going intermediate-frequency (IF) carriers assigned to the same satellite repeater into one composite signal. A DCPA-driver amplifier controls the level of each composite IF signal in accordance with the current total loading of each repeater. Each DCPA driver amplifier associated with one of the IF signals has a controllable gain function. For satellite communications systems employing a single feeder earth station, the gain-control function of each driver amplifier is preferably performed automatically. When the total traffic loading for a repeater is above a predetermined or adjustable threshold, the associated driver amplifier automatically selects a gain position that corresponds to a zero relative gain with respect to the nominal value needed for 100% full-load conditions, i.e. no additional gain or boost is provided. When the loading is below the threshold, the driver amplifier automatically selects a fixed gain point which is a predetermined amount above the zero-relative gain, i.e. the gain is increased based on reduced system loading for that particular repeater. The driver amplifier operates in this gain position while the traffic loading is below the threshold point. In this manner, all active carriers passing through the amplifier receive a fixed boost to their power levels. This in turn results in a corresponding increase when the carriers pass through the HPA assembly of the feeder earth station. The increased uplink level results in a corresponding increase to the downlink power of each affected carrier passing through the satellite repeater which results in improved power utilization to enhance system performance.

A method is also provided to improve power utilization and increase efficiency for communication systems where multiple feeder earth stations are employed, all of which may load the same satellite repeaters. The method controls the aggregate power level of uplink signals in a similar manner as that described above for the single earth feeder station implementation. However, where multiple earth feeder stations are employed, the gain-control function of each DCPA-driver amplifier is determined by a Network Demand-assigned multiple-access Control Center (NDCC). The NDCC centrally manages the overall or aggregate traffic assignment and loading of each satellite repeater through its interactions with all of the feeder earth stations. Thus, the NDCC is aware of the total loading of each satellite repeater imposed by all of the feeder earth stations and selects a common gain position for the DCPA-driver amplifiers of all feeder earth stations accordingly. The NDCC preferably communicates with each feeder station at all times to perform this function.

The present invention groups individual user carriers based on the intended satellite repeater rather than grouping by user location as in the prior art systems. After grouping according to the intended repeater, each composite IF signal is passed through a DCPA driver amplifier module for level control as described above. The output of all the DCPA driver amplifier modules are then combined into a single composite signal and fed to the upconverter-HPA subsystem as in the existing systems. The particular DCPA configuration is determined on a case-by-case basis depending on the configuration details of the existing network. Generally, the DCPA configuration includes a number of DCPA driver amplifier modules, signal dividers, band-pass filters, and combiners as explained in greater detail below.

For all new systems, the present invention may be implemented as part of each satellite repeater in the form of a DCPA-Driver amplifier replacing the traditional driver amplifier which precedes the HPA unit for the repeater. In such systems the DCPA-Driver amplifier automatically controls the gain as described with respect to the single-feeder station case for a ground-based implementation.

The present invention has a number of advantages relative to the prior art systems and methods. The present invention better utilizes the downlink power of repeaters under all loading conditions resulting in an increase in the downlink power for each carrier under reduced traffic loading conditions. This increase in downlink power results in a corresponding increase in the downlink margin. As a result, the communication link has a higher availability when compared to the link availability achievable under the lower fixed power systems of the prior art. To achieve the same higher average link availability using traditional methods, more downlink power would have to be allocated to each carrier resulting in an increase in the total required repeater power and therefore the total satellite power at additional cost, if available at all. Thus, the present invention is analogous to an increase of the satellite power which is manifested in various system benefits to improve overall system performance—without the attendant disadvantages of increased cost and weight.

For new systems, the resulting benefits of the present invention can be directly applied to reduce the required satellite payload power for a particular mission thereby resulting in reduced costs. For existing systems, advantages of the present invention include increasing the total number of carriers supported by the system (if additional frequency spectrum is available), increasing the average link margin and availability of communications services, increasing the system coverage and service area (when combined with an upgrade of the radiated power of the end user stations), or any combination thereof as determined by the system owner and operator.

The above objects and other objects, features and advantages of the present invention will be readily appreciated by one of ordinary skill in the art from the following detailed description of the best modes for carrying out the invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a general configuration for a satellite communication system with which the present invention may be integrated;

FIG. 2 is a block diagram representation showing integration of DCPA assemblies into feeder earth stations according to the present invention for a ground-based implementation;

FIG. 3 is a block diagram illustrating details of a Dynamic Carrier Power Allocation (DCPA) Assembly for a ground-based implementation of the present invention;

FIG. 4 is a block diagram illustrating a DCPA-driver amplifier module according to the present invention; and

FIG. 5 is a flow chart illustrating a method for improving utilization of satellite payload power according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring to FIG. 1, a satellite communication system **10** is illustrated. Satellite communication system **10** includes a plurality of feeder earth stations **12** located on Earth. Feeder earth stations **12** transmit signals to a satellite **16** in an orbit around Earth. Satellite **16** includes at least one repeater **18** which receives signals from feeder earth stations **12**, processes the signals, changes their frequency, and transmits the signals to one or more end user stations (EUS) **20** located on Earth. Satellite **16** may transmit signals using a single beam or multiple beams each supported by a single or an aggregate of repeater sections depending upon the particular application.

Feeder earth stations **12** are preferably fixed in location. End user stations **20** may be fixed, portable, or mobile. Each feeder earth station **12** has an antenna **22** for transmission of signals via carriers of suitable frequencies to a receiving antenna **26** of satellite **16**. Each end user station **20** has an antenna **28** for reception of the signals transmitted via suitable carriers from a transmitting antenna **32** of satellite **16**. In most applications, the same antenna may be used for both transmitting and receiving signals.

One or more repeaters **18** (best illustrated in FIG. **2**) are connected between receiving antenna **26** and transmitting antenna **32**. The present invention may be used in a variety of communication applications. For example, satellite communication system **10** may be employed for the transmission of telephonic and data signals. Private or public telephone and data networks **36** may connect with one or more of feeder earth stations **12**. A network DAMA and control center (NDCC) **40** may be used to monitor and control the communications traffic of feeder earth stations **12** as explained in greater detail below.

Referring now to FIG. **2**, a block diagram of various components of communication system **10** illustrates use of Dynamic Carrier Power Allocation (DCPA) according to the present invention. Preferably, satellite communication system **10** uses a multi-carrier per repeater, demand-assigned transmission architecture. All signal carrier frequency/channel assignments to feeder stations **12** and end-user stations **20**, in addition to system loading, are managed and controlled by NDCC **40**. Communication system **10** may have only a single feeder earth station **12** in which case NDCC **40** functionalities may be incorporated into the feeder earth station.

Feeder earth stations **12** transmit signals to end user stations **20** via one or more repeater sections **18** (numbered one through "m") of satellite **16**. Satellite **16** receives uplink signals via receiving antenna **26** and allocates them to one or more repeater sections **18** based on the carrier frequency of the signal. Each repeater section **18** converts the signals to a downlink frequency and may use a fixed gain amplifier to prepare the signal for retransmission via one or more beams to end user stations **20**. One of ordinary skill in the art will recognize that the blocks representing satellite repeaters **18** as shown in FIG. **2** are only functional representations for convenience and ease of illustration. Of course, in practice many payload subsystems, including receive and transmit antennas, receivers, HPA assemblies, and the like, could be shared by several conceptual repeaters.

Where more than one feeder earth station **12** is employed in communication system **10**, traffic loading coordination among feeder earth stations **12** is provided by NDCC **40**. Each feeder earth station **12** includes Network Interface Equipment **44** through which feeder earth stations **12** interface with network **36**. Each feeder earth station **12** further includes a plurality of channel units (CU) **46**. Channel units **46** process and modulate user information signals into intermediate-frequency (IF) signals for transmission, in addition to demodulating received IF signals to recover user information. As such, the number of channel units **46** in operation and active at any particular time depends upon the traffic loading of communication system **10**. During off-peak hours, only a few of channel units **46** will actually be active at any one time.

Signal carriers from feeder earth stations **12** corresponding to channel units **46** are transmitted to satellite **16** and after reception are passed to various repeater sections **18**. Each channel unit **46** is dynamically assigned by NDCC **40** to work through a designated repeater section **18** according to a predetermined carrier frequency plan. Feeder earth stations **12** further include a signal combiner **48**, coupled to channel units **46**, for combining the modulated IF signals. The combined or composite signal is communicated to Dynamic Carrier Power allocation (DCPA) assembly **50**, an upconverter (U/C) **52**, and a high-power amplifier (HPA) **54**.

FIG. **3** illustrates a generic block diagram for implementation of the DCPA system and method according to the present invention for satellite systems that have already been deployed and are in operation. One embodiment of the present invention may be implemented by the integration of DCPA Assembly **50** into the feeder earth station(s) as shown. DCPA Assembly **50** includes a power divider or splitter **60**, a plurality of sets **62** of band pass filters **64**, a plurality of signal combiners **66**, a plurality of DCPA modules **68**, and a signal combiner **70**.

In operation, the combined IF signal from combiner **48** (FIG. **2**) is divided by power divider **60** among band pass filters **64**. Within a feeder earth station **12**, the passbands of filters **64** differ from each other so that each band pass filter **64** separates a portion of the total IF spectrum, in effect separating a number of the individual IF carriers. As such, the plurality of filter groups **62** separates and groups together all those IF carriers (component signals) which will be retransmitted by the same satellite repeater section **18**. Combiners **66** combine the outputs of all the associated band pass filters **64** of a filter set **62** corresponding to a particular repeater section **18** to form a composite IF signal. Filters **64** are labeled 1—1 through 1-j, and m-1 through m-j, where the first number represents a designated repeater section and the second number represents the particular spectral band of the filter.

The output of each combiner **66** (i.e, composite IF signal for a particular repeater) will vary depending upon the number of active channel units **46** designated for a particular repeater section **18**. After being combined by a corresponding signal combiner **66**, each composite IF signal is amplified by a corresponding DCPA module **68** described in greater detail with reference to FIGS. **4** and **5**. For systems with a single feeder earth station, DCPA modules **68** operate autonomously to control the gain applied to the signals based on the current loading of each repeater section. For

systems with multiple feeder stations, DCPA modules **68** operate under the control of the system NDCC through commands **80** as explained in greater detail with reference to FIG. **4**.

Output signals of DCPA modules **68** are then combined by combiner **70** to produce another composite IF signal which is applied to upconverter **52** and high power amplifier **54** (best illustrated in FIG. 2). Preferably, HPA **54** operates in a multi-carrier, linear mode to amplify the resulting composite signal (composed of multiple IF signals) to a power level suitable for transmission via antenna **22** to one or more repeaters **18** of satellite **16**. Each repeater **18** receives a portion of the uplink signals having frequencies falling within its predetermined frequency range. The signals are then amplified and converted to downlink frequency signals for re-transmission via antenna **32** to end user stations **20**. Other than the modifications to implement the DCPA as described above, the remaining functions of the feeder stations are performed in the traditional manner.

In the prior art communication systems, every IF signal from every channel unit in each feeder earth station is treated equally and is allocated a fixed amount of power amplification from the HPA's regardless of how many other carriers are present at the time. The end-to-end link through each satellite repeater is engineered accordingly to deliver the required performance as if each repeater is 100% loaded with traffic so the repeater power would be fully exhausted. When the traffic loading is not at 100%, each carrier still transmits to the satellite with the same fixed level. Being a linear channel end-to-end, only a fraction of the repeater power in proportion to the number of uplinked carriers is utilized, with the remainder of the power being left idle.

According to the present invention, each DCPA module **68** (in a system with a single feeder earth station) monitors the loading condition of its associated repeater and automatically chooses its operating gain position accordingly. For best system performance the DCPA module is preferably implemented with a bi-modal gain capability. A first operating point corresponds to a loading range between a predetermined DCPA threshold and a point representing 100% loading. This point may be referred to as the zero relative gain point because the present invention preferably provides no additional gain when loading is within this range. While the traffic loading is below the DCPA threshold, a fixed relative gain is applied to all signals assigned to that particular repeater. To avoid operational degradations, the DCPA threshold level should preferably be kept within a range of about 40–70% of the full loading conditions. For any particular operating point, the DCPA module operates like a fixed-gain amplifier. As long as the transponder/repeater loading conditions are below the threshold level, the DCPA module increases the level of every associated carrier by a selectable constant DCPA gain amount, regardless of the actual level of the total loading.

As an example, with a DCPA threshold value of 50%, the DCPA module will provide a fixed relative gain, such as 3 Db, when the total loading in a particular repeater is below 50% of its maximum value. This additional gain will be provided as long as the total loading stays below the DCPA threshold level (50% in this example). As such, the DCPA module increases the level of every associated IF signal by a fixed 3 dB amount. This increase will directly result in a corresponding 3 dB increase in power by the associated HPA which transmits the carriers to the satellite. For non-regenerative satellite payloads, this in turn will drive the repeater proportionately higher and result in a 3 dB increase in the transmitted power of the downlink for each carrier. When the traffic loading for the associated repeater exceeds the threshold level, the DCPA module returns to the zero relative gain operation which corresponds to the gain for full load conditions. In this manner the DCPA module of the present invention imparts at least some (or all) of the unused transponder power to the signal carriers present to improve system performance.

FIG. **4** is a functional block diagram illustrating a DCPA module according to the present invention. The DCPA module illustrated may be used in both ground-based and satellite-based applications. DCPA module **68** includes a selectable-gain amplifier **82** which receives its input from one of the signal combiners **66**. DCPA module **68** also includes a detector **84**, a reference signal source **86**, comparator logic **88**, and a command receiver **90**. The composite input signal from combiner **66** represents one set of signal carriers passing through a particular satellite repeater which is amplified by amplifier **82**, the output of which is continuously sampled by detector **84**. The output of detector **84** is applied to comparator logic **88** which compares it to a reference value generated by reference source **86**. The reference value preferably represents the 100% traffic loading conditions for the associated repeater. The reference value may be modified by a calibration **94** generated by command receiver **90** in response to a an NDCC command **80** for those systems utilizing multiple feeder stations and a NDCC. Comparator logic **88** determines its output based on the inputs from detector **84** and reference source **86** according to a loading algorithm based on the particular application.

Preferably, before any one of the satellite repeaters is put into service, power is applied to the associated DCPA modules (whether part of the repeater on the satellite or part of the feeder earth station on the ground). After performing a self-test and initialization, the DCPA module is configured for an appropriate full-load (zero relative) gain and DCPA threshold gain based on a predetermined DCPA threshold loading value. Because there is no traffic (and therefore no input signal from combiner **66**), there is also no output from DCPA amplifier **82**. Detector **84** gives a no-output value to comparator logic **88** which compares this signal with the output from reference source **86**. Since the traffic loading is below the DCPA threshold, comparator logic **88** selects the DCPA threshold gain as the initial operating state for amplifier **82**. For most systems the relative gain applied when the traffic is below the DCPA threshold is preferably in a range of about 2 to 4 dB above the gain value for full-load conditions.

Assuming a 3 dB relative gain at the time of initial configuration, DCPA module **68** will increase the power level of every signal carrier passing through it by 3 dB. This will continue as long as the output power of amplifier **82** (as monitored by detector **84**), remains at least 3 dB below the full-load power value. The relative gain is in addition to the gain that would normally be applied to each carrier to properly drive the associated HPA assembly under full-load conditions. When the total loading in the associated repeater approaches the DCPA threshold value (50% in this example), the power output of amplifier **82** will approach the full-load power level represented by reference source **86**. At this point, comparator logic **88** commands amplifier **82** to switch to the zero relative gain state, lowering the carriers back to their nominal (non-DCPA aided) values. This eliminates the possibility of over-driving the repeater HPA assembly and attendant signal degradations as traffic loading continues to increase past the threshold level.

The zero relative gain state continues until the repeater loading reverses direction and drops below the DCPA

threshold, at which point amplifier **82** is commanded to change to the DCPA relative gain (3 dB) state. Operation continues in this manner automatically and indefinitely in response to the current traffic loading conditions. Of course, sufficient hysteresis is preferably built into the control loop to prevent unnecessary switchings between the gain states. As such, the embedded software and intelligent algorithm of the comparator logic sub-unit should be carefully designed to achieve reliable and stable operation of the DCPA-Driver amplifier.

For ground-based implementations with multiple feeder stations, the operation of DCPA module **68** is under direct control of NDCC **40** through NDCC commands **80**. For these applications, comparator logic **88** is placed in a manual mode where it follows the NDCC commands **80** to set the gain of amplifier **82**. The NDCC generates commands for DCPA module **68** based on the traffic loading conditions of a particular repeater which may originate from one or more of the feeder earth stations **12**. As such, the NDCC selects either the zero relative gain or the DCPA threshold gain based on the DCPA loading threshold of each associated repeater. As described above, prior art systems typically proportionately allocate payload power among the repeater sections and the signal carriers assuming a full-load condition, i.e. the maximum number of carriers are present. During off-peak hours, much of the available payload power is unused and left idle. According to the present invention, this available idle power may be used to improve the quality of service and link availability for those carriers that are actually in use. This is accomplished by the ground-based DCPA which provides for more efficient use of the expensive satellite payload power.

For new systems or those that are in the design and construction stage, the present invention can be integrated with the satellite payload. In such cases the traditional driver amplifier module preceding every HPA amplifier assembly will be replaced by a new DCPA-Driver amplifier module. While traditional driver amplifiers working with single-carrier-saturated transponders employ a measure of automatic-gain-control to keep the HPA driven to saturation against a limited amount of uplink signal attenuations, all multi-carrier demand-assigned satellite systems (as the target of the present invention) operate each repeater or transponder in a linear mode below saturation. In such cases, the driver amplifier cannot be used to react to variations in the level of many uncorrelated input carriers. Therefore, the multi-carrier demand-assigned systems must utilize a single fixed gain at all times for proper operation of the system. The DCPA-driver amplifier module of the present invention will in effect operate with a special gain-control function having a gain value which is determined not by variations in the received level of the collective or individual carriers, but based on the instantaneous loading conditions relative to the maximum permissible loading level. Under nominal conditions, operation of the satellite-based DCPA-Driver amplifier is fully automatic and is done without any input from the NDCC, regardless of the particular ground segment configuration. However, to provide for more accurate operation, and to provide a measure of choice and control in selection of different threshold level values, the driver amplifier module is preferably equipped with both a calibration and a gain-selection capability. The NDCC gain-set command **92** may be used to: (a) disable the DCPA function by resetting the amplifier to its nominal gain position, and (b) select a different DCPA threshold level. Through calibration command **94**, DCPA-driver amplifier module **68** can be calibrated for the accuracy of reference source **86** and its overall gain for optimum performance. As will be appreciated by one of ordinary skill in the art, the satellite-based version of DCPA-driver amplifier module **68** is generally designed for RF frequencies rather than the much lower IF frequencies for the ground-based version.

In many satellite systems, the return transmissions from all individual end-user stations back to the feeder earth station(s) will go through one or more satellite repeaters under similar conditions as discussed for the forward direction. In such cases, the return repeater is also sized for its power rating under the full traffic loading conditions. The DCPA of the present invention can also be employed with such repeaters but only as part of the satellite repeater. Similar benefits in terms of improved link quality and availability will also be realized in such cases. A ground-based implementation for the return direction would be very difficult, if at all possible, as the return carriers are transmitted by thousands of end-user stations on an individual basis. As such, the only point where they are accessible as a set is in the satellite.

FIG. **5** illustrates an alternative representation for a system and method of improving utilization of satellite payload power according to the present invention. As will be appreciated by one of ordinary skill in the art, the various functions illustrated in FIG. **5** may be performed in appropriate hardware, software, or a combination thereof. The system and method is illustrated in a consecutive fashion for convenience only. As such, the order of the functions illustrated may not be necessary to accomplish the objects, features, and advantages of the present invention.

Block **100** of FIG. **5** represents grouping of a variable number of user carriers into at least one group of signals corresponding to each satellite repeater. Each group forms a first combined signal which has an associated aggregate signal level. As illustrated and described with reference to FIGS. **1–4**, grouping may be performed by filtering the user carriers to generate component signals based on predetermined frequency ranges associated with each repeater, as represented by block **102**. When those applications employ more than one feeder earth station, block **100** may include grouping user carriers from all of the feeder earth stations and the corresponding groups where each group corresponds to one of the satellite repeaters, as represented by block **104**.

The current loading for each repeater is determined as represented by block **106**. If the aggregate loading across all feeder stations for a particular repeater is less than a threshold as represented by block **108**, the DCPA gain is applied as represented by block **110**. If the current loading for a repeater is above the threshold (with appropriate hysteresis), the additional gain is not applied. Rather, the nominal gain is applied to the signal as represented by block **112**. To determine whether the aggregate loading for a particular repeater is greater than the predetermined or adjustable threshold, the combined signal may be compared to a corresponding reference signal as described and illustrated in detail above. When the reference signal exceeds a signal representing the aggregate loading level for a repeater, a predetermined gain is applied as represented by block **110**. Note that the nominal gain, represented by block **112**, is applied whether or not the increased gain is applied. As such, block **112** represents a zero-relative gain or nominal gain.

The amplified signals are combined to form a second combined signal for transmission to or from the satellite as represented by block **114**. The combined signal is then transmitted via the satellite, as represented by block **116**. For ground-based implementations, the functions represented in

FIG. 5 would be performed within the feeder earth station. Of course, for satellite implementations, the functions of FIG. 5 would be performed by the satellite.

It is to be understood, of course, that while the forms of the present invention described in this document constitute the preferred embodiments of the present invention, the descriptions are not intended to illustrate all possible forms thereof. It is also to be understood that the words used are words of description, rather than limitation, and that in actual practice various changes may be made to meet the needs of every system without departing from the spirit and scope of the present invention, which should be construed according to the following claims.

What is claimed is:

1. A system for improving utilization of satellite payload power in a communication system having at least one uplink signal representing a variable number of user carriers, the uplink signal being transmitted from at least one feeder earth station to at least one end user station via a satellite having at least one repeater, the system comprising:

a splitter to divide the uplink signal into at least one group corresponding to each repeater;

at least one filter set corresponding to each group, the filter set being in communication with the splitter to separate the variable number of carriers by frequency bands corresponding to each group;

at least one combiner in communication with a corresponding filter set for combining carriers associated with each repeater to produce an aggregate signal; and

at least one amplifier in communication with a corresponding combiner, the amplifier having a controllable gain based on the aggregate signal such that the gain is increased when the aggregate signal level is below an associated threshold to improve power utilization in the corresponding repeater.

2. The system of claim 1 further comprising:

a signal combiner in communication with all the amplifiers for generating a composite signal.

3. The system of claim 1 wherein the at least one feeder earth station includes a plurality of feeder earth stations, the system further comprising:

a central network controller in communication with the amplifiers for controlling gain of each amplifier based on an aggregate traffic load of the plurality of feeder earth stations corresponding to each repeater.

4. The system of claim 3 wherein the central network controller increases the gain of each amplifier which is below the threshold by about two to four decibels.

5. The system of claim 1 wherein each amplifier applies a nominal gain to the aggregate signal when the aggregate signal is above the threshold and an increased gain when the aggregate signal is below the threshold.

6. The system of claim 1 wherein each of the at least one amplifier comprises:

a detector for sampling output of a corresponding amplifier and generating an output level signal in response thereto;

a reference source for providing a reference signal indicative of a desired level corresponding to the full-load output of the amplifier;

a comparator for comparing the output level signal and the reference signal and generating a gain control signal in response thereto, the gain control signal controlling the gain of the amplifier; and

a command receiver for receiving signals from a central network control center to control the gain of the amplifier according to traffic loading by the feeder earth stations.

7. The system of claim 1 wherein the at least one splitter, the at least one filter set, the at least one combiner, and the at least one amplifier are disposed within a satellite.

8. A method for improving utilization of satellite payload power in a communication system using at least one uplink signal representing a variable number of user carriers, the uplink signal being transmitted from at least one feeder earth station to at least one end user station via a satellite having at least one repeater, the method comprising:

grouping the variable number of user carriers into at least one group of signals corresponding to each repeater, each group forming a first combined signal having an associated aggregate signal level;

amplifying each first combined signal having an aggregate signal level below a threshold level; and

combining the at least one group of signals to form a second combined signal for transmission via the satellite.

9. The method of claim 8 wherein the step of grouping comprises:

filtering the user carriers to generate a plurality of component signals based on a corresponding plurality of predetermined frequency ranges associated with each repeater.

10. The method of claim 8 wherein the at least one feeder earth station comprises a plurality of feeder earth stations and wherein the step of grouping comprises:

grouping user carriers from all of the plurality of feeder earth stations into a plurality of groups, each group corresponding to one repeater.

11. The method of claim 8 wherein the step of amplifying comprises:

comparing each first combined signal to a corresponding reference signal; and

applying a predetermined gain to each first combined signal having a corresponding reference signal which exceeds the aggregate signal level of the first combined signal.

* * * * *

US005783969A

United States Patent [19]

Luz

[11] Patent Number: 5,783,969

[45] Date of Patent: Jul. 21, 1998

[54] **METHOD AND SYSTEM FOR PREVENTING AN AMPLIFIER OVERLOAD CONDITION IN A HYBRID MATRIX AMPLIFIER ARRAY**

[75] Inventor: **Yuda Yehuda Luz**, Euless, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **708,864**

[22] Filed: **Sep. 4, 1996**

[51] Int. Cl.[6] **H03F 3/68**

[52] U.S. Cl. ..... **330/124 R**; 330/207 P

[58] Field of Search ..... 330/53, 124 D, 330/124 R, 207 D, 286, 295, 298

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,732,217	5/1973	Gorset et al.	330/56
5,604,462	2/1997	Gans et al.	330/124 R
5,610,556	3/1997	Rabin	330/295 X
5,638,024	6/1997	Dent et al.	330/124 R

OTHER PUBLICATIONS

Sandrin, W.A., "The Butler Matrix Transponder", Comstat Technical Review, vol. 4, No. 2, Fall 1974, pp. 319-344.

Meredith, Sheldon, presentation on Cellwave Smart System at "Second Annual Workshop on Smart Antennas in Wireless Mobile Communications", Jul. 20-21, 1995, Stanford University.

Gerst, Carl, W., "Hybrid Matrix Amplifiers", An Anaren White Paper, Nov. 1995.

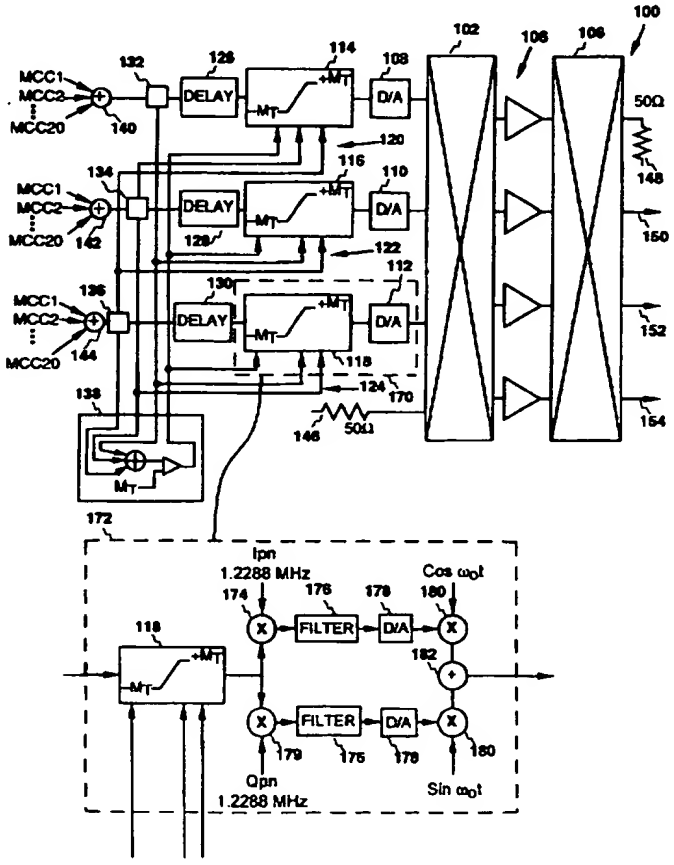
Primary Examiner—Steven Mottola

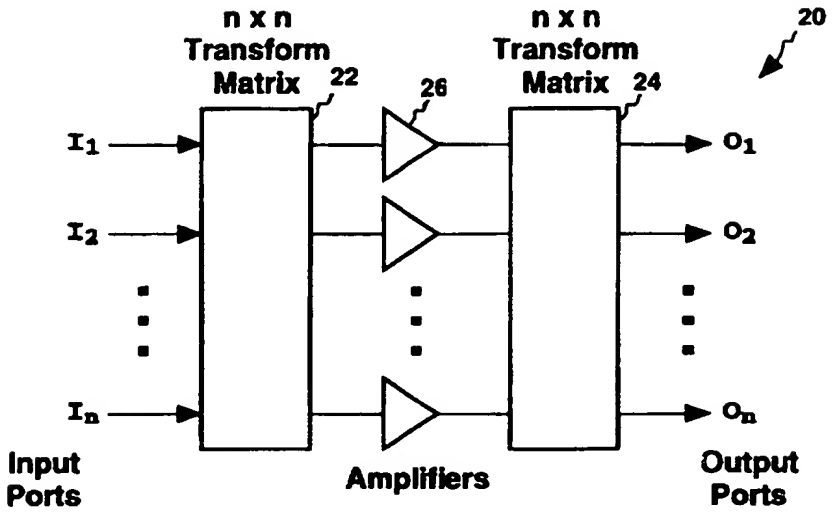
Attorney, Agent, or Firm—Bruce Terry

[57] **ABSTRACT**

In a hybrid matrix amplifier array (**100**), the amplitude of each of a plurality of input signals is measured (**132–136, 202**). In response to the signal amplitude measurements, an overload condition that will result in an amplifier overload in said hybrid matrix amplifier array is estimated (**204, 206, 138**). In response to the estimation of the overload condition, the signal amplitude of at least one of the plurality of input signals is modified to prevent the overload condition in the hybrid matrix amplifier array. An overload condition may be estimated if the sum of the amplitudes of the input signals exceeds a threshold (**206**). In one embodiment, all input signals are modified by proportionately reducing the amplitude of each of the plurality of input signals (**304**).

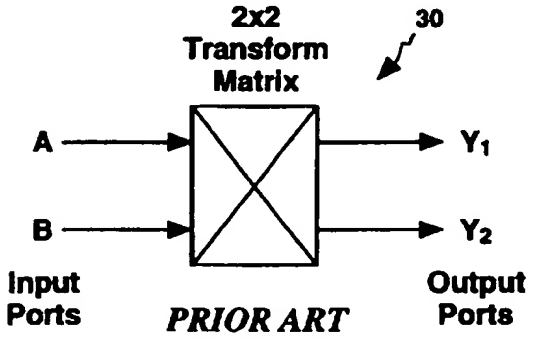
19 Claims, 7 Drawing Sheets





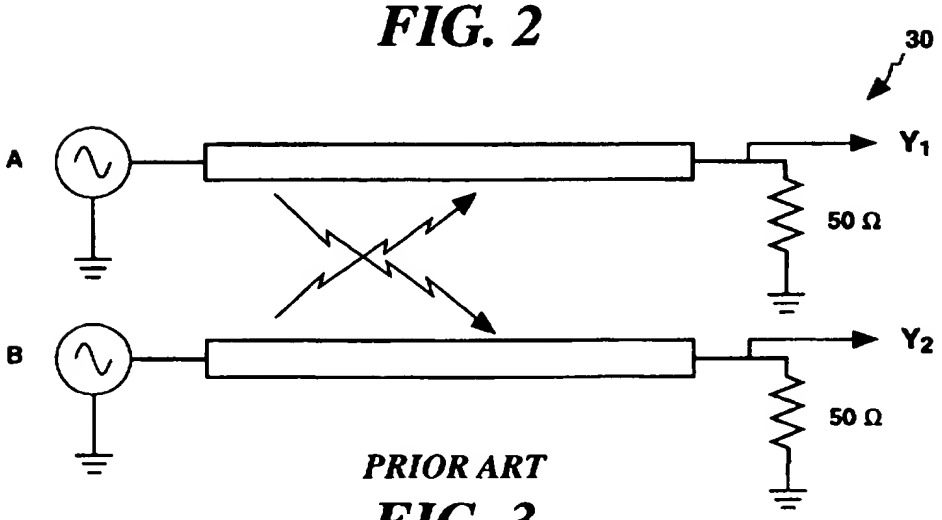
PRIOR ART

FIG. 1



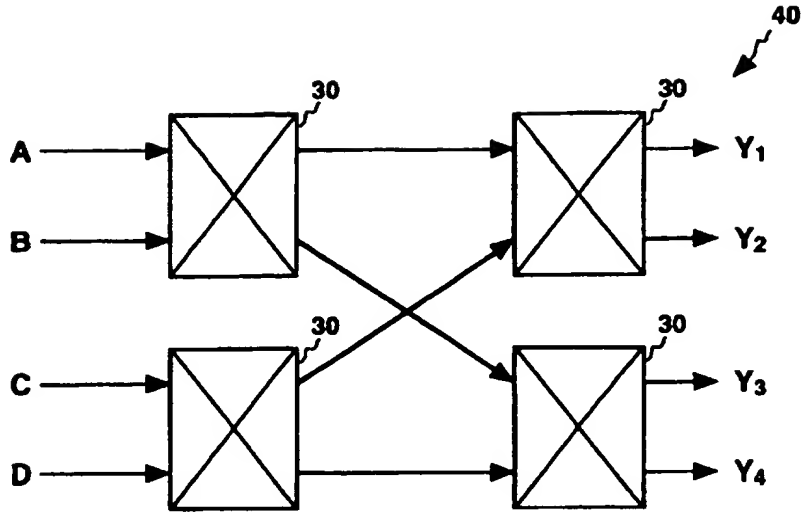
PRIOR ART

FIG. 2



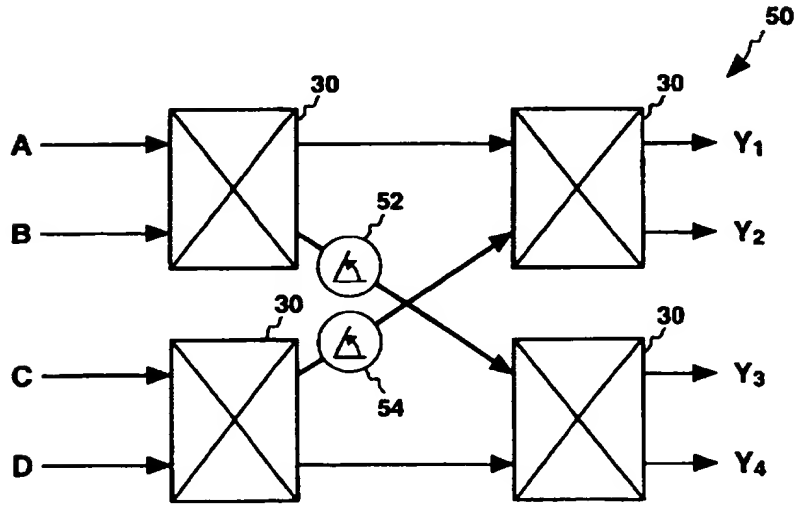
PRIOR ART

FIG. 3



PRIOR ART

FIG. 4



PRIOR ART

FIG. 5

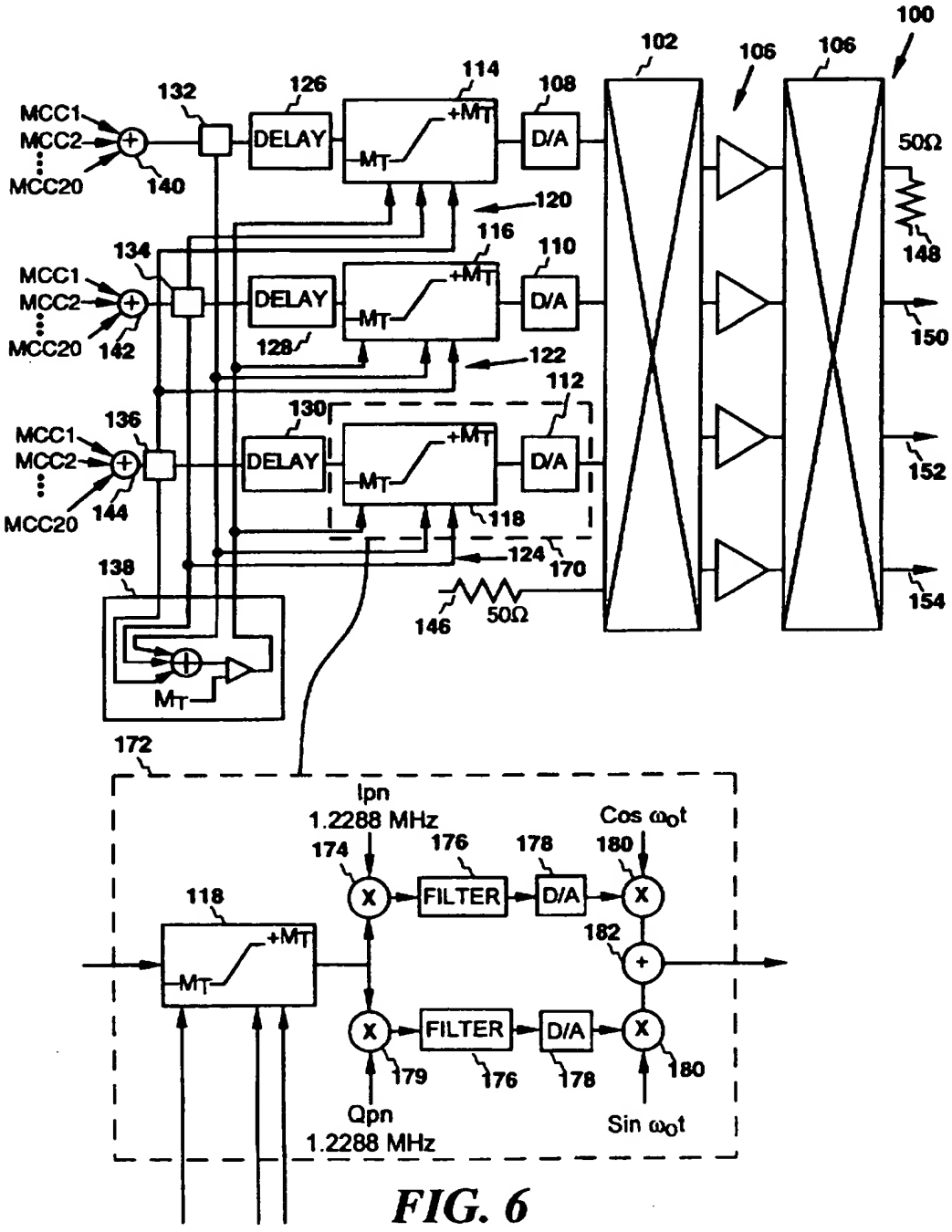

100
102
106
106
MCC1
MCC2
MCC20
132
140
126
DELAY
114
+MT
MT
108
D/A
120
50Ω
148
134
142
116
110
128
122
150
112
130
136
144
118
124
170
138
146
50Ω
152
154
172
Ipn
1.2288 MHz
Cos ωot
174
176
178
180
FILTER
182
179
Qpn
1.2288 MHz
Sin ωot

FIG. 6

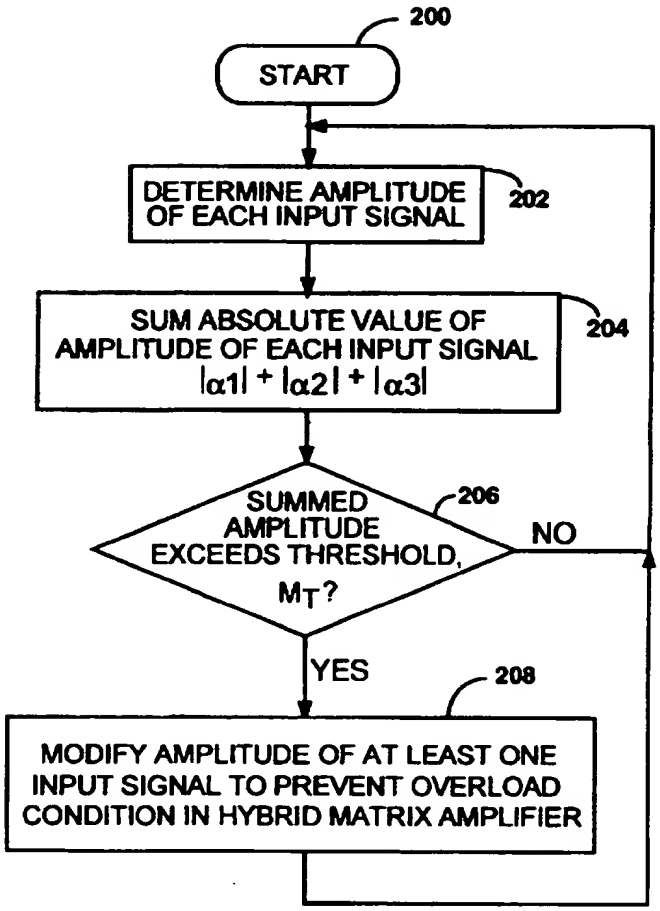

200
START
DETERMINE AMPLITUDE OF EACH INPUT SIGNAL
202
SUM ABSOLUTE VALUE OF AMPLITUDE OF EACH INPUT SIGNAL
|α1| + |α2| + |α3|
204
SUMMED AMPLITUDE EXCEEDS THRESHOLD, MT?
206
NO
YES
208
MODIFY AMPLITUDE OF AT LEAST ONE INPUT SIGNAL TO PREVENT OVERLOAD CONDITION IN HYBRID MATRIX AMPLIFIER

FIG. 7

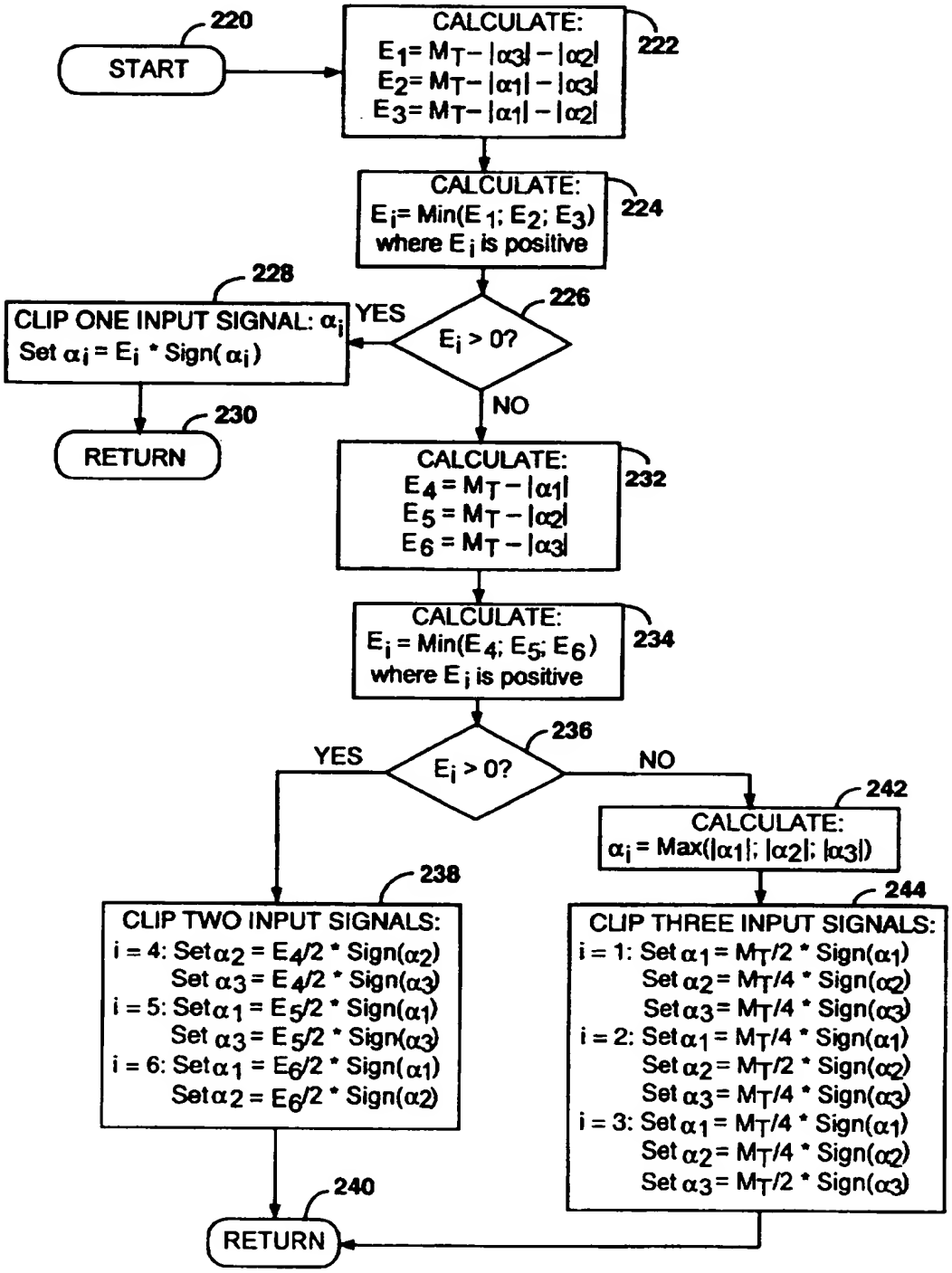

220
START
CALCULATE:
$E_1 = M_T - |\alpha_3| - |\alpha_2|$
$E_2 = M_T - |\alpha_1| - |\alpha_3|$
$E_3 = M_T - |\alpha_1| - |\alpha_2|$
222
CALCULATE:
$E_i = \text{Min}(E_1; E_2; E_3)$
where E_i is positive
224
226
$E_i > 0$?
YES
228
CLIP ONE INPUT SIGNAL: α_i
Set $\alpha_i = E_i * \text{Sign}(\alpha_i)$
230
RETURN
NO
CALCULATE:
$E_4 = M_T - |\alpha_1|$
$E_5 = M_T - |\alpha_2|$
$E_6 = M_T - |\alpha_3|$
232
CALCULATE:
$E_i = \text{Min}(E_4; E_5; E_6)$
where E_i is positive
234
236
$E_i > 0$?
YES
NO
238
CLIP TWO INPUT SIGNALS:
i = 4: Set $\alpha_2 = E_4/2 * \text{Sign}(\alpha_2)$
Set $\alpha_3 = E_4/2 * \text{Sign}(\alpha_3)$
i = 5: Set $\alpha_1 = E_5/2 * \text{Sign}(\alpha_1)$
Set $\alpha_3 = E_5/2 * \text{Sign}(\alpha_3)$
i = 6: Set $\alpha_1 = E_6/2 * \text{Sign}(\alpha_1)$
Set $\alpha_2 = E_6/2 * \text{Sign}(\alpha_2)$
240
RETURN
242
CALCULATE:
$\alpha_i = \text{Max}(|\alpha_1|; |\alpha_2|; |\alpha_3|)$
244
CLIP THREE INPUT SIGNALS:
i = 1: Set $\alpha_1 = M_T/2 * \text{Sign}(\alpha_1)$
Set $\alpha_2 = M_T/4 * \text{Sign}(\alpha_2)$
Set $\alpha_3 = M_T/4 * \text{Sign}(\alpha_3)$
i = 2: Set $\alpha_1 = M_T/4 * \text{Sign}(\alpha_1)$
Set $\alpha_2 = M_T/2 * \text{Sign}(\alpha_2)$
Set $\alpha_3 = M_T/4 * \text{Sign}(\alpha_3)$
i = 3: Set $\alpha_1 = M_T/4 * \text{Sign}(\alpha_1)$
Set $\alpha_2 = M_T/4 * \text{Sign}(\alpha_2)$
Set $\alpha_3 = M_T/2 * \text{Sign}(\alpha_3)$

FIG. 8

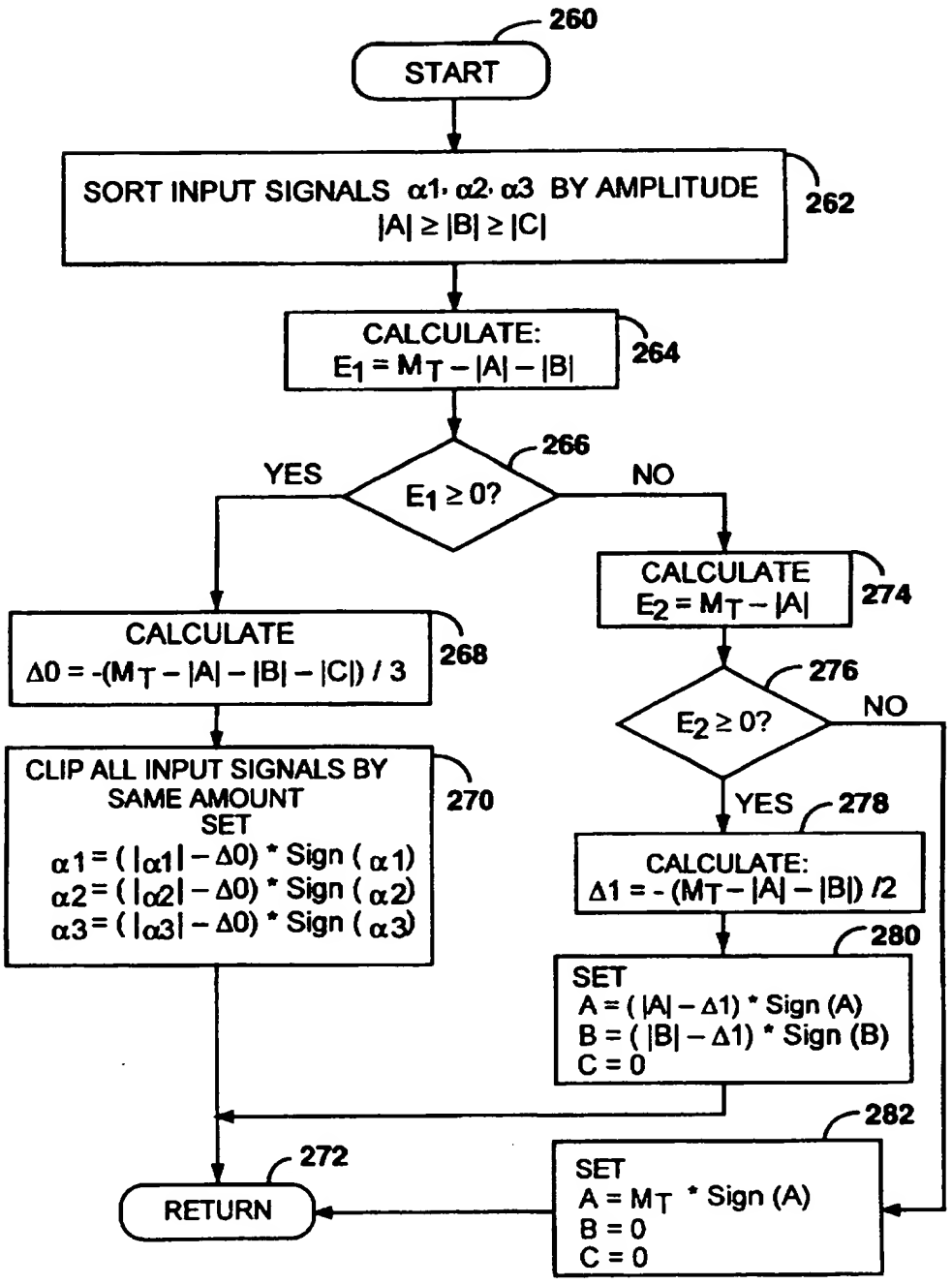

260
START
SORT INPUT SIGNALS α1, α2, α3 BY AMPLITUDE
|A| ≥ |B| ≥ |C|
262
CALCULATE:
E1 = MT – |A| – |B|
264
266
E1 ≥ 0?
YES
NO
CALCULATE
Δ0 = -(MT – |A| – |B| – |C|) / 3
268
CLIP ALL INPUT SIGNALS BY SAME AMOUNT
SET
α1 = (|α1| – Δ0) * Sign (α1)
α2 = (|α2| – Δ0) * Sign (α2)
α3 = (|α3| – Δ0) * Sign (α3)
270
CALCULATE
E2 = MT – |A|
274
276
E2 ≥ 0?
NO
YES
278
CALCULATE:
Δ1 = - (MT – |A| – |B|) /2
280
SET
A = (|A| – Δ1) * Sign (A)
B = (|B| – Δ1) * Sign (B)
C = 0
282
SET
A = MT * Sign (A)
B = 0
C = 0
272
RETURN

FIG. 9

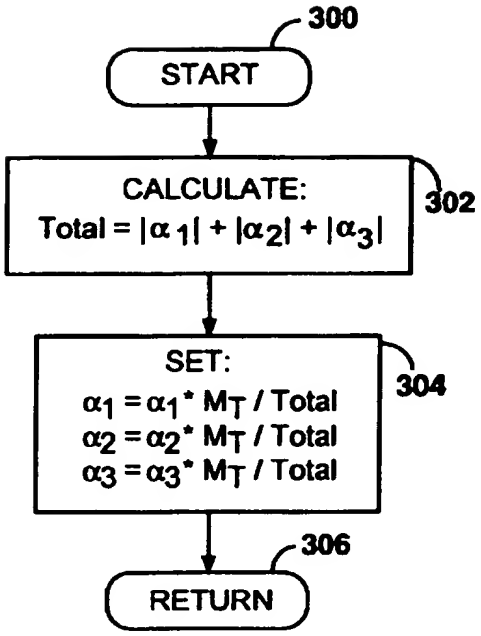

300
START
CALCULATE:
Total = |α1| + |α2| + |α3|
302
SET:
α1 = α1* MT / Total
α2 = α2* MT / Total
α3 = α3* MT / Total
304
306
RETURN

FIG. 10

METHOD AND SYSTEM FOR PREVENTING AN AMPLIFIER OVERLOAD CONDITION IN A HYBRID MATRIX AMPLIFIER ARRAY

FIELD OF THE INVENTION

The present invention is related in general to signal amplification, and more particularly to an improved method and system for preventing an amplifier overload condition in a hybrid matrix amplifier array.

BACKGROUND OF THE INVENTION

A hybrid matrix amplifier is a parallel set of amplifiers, each having inputs fed, and outputs combined, with multi-port matrices made up of hybrid couplers. The general configuration of a hybrid matrix amplifier **20** is shown in FIG. **1**. Hybrid matrices **22** and **24** connected in the manner shown create information paths—extending from I_n to O_n—which are separate at the input ports I_n and output ports O_n. Between hybrid matrices **22** and **24** amplifier array **26** is used to amplify signals. These signals between the matrices are distributed evenly in amplitude, and have a specific phase relationship according to which input port I_n the signal entered. When amplifier array **26** is configured between matrices **22** and **24**, all amplifiers in amplifier array **26** share the amplification of the signal on the path I_1 to O_1, as well as signals on all other n−1 paths.

A basic building block of many transform matrices is a 90° hybrid- or 3 dB coupler, which is shown schematically in FIG. **2** as coupler **30**. Coupler **30** has four ports: two input ports, A and B, and two output ports, Y_1 and Y_2. Coupler **30** is typically linear and reciprocal. Because of the reciprocal nature of coupler **30**, input ports A and B can be interchanged with output ports Y_1 and Y_2. The coupler also has a given characteristic bandpass and characteristic impedances at the ports.

In operation, if signal A is received at input port A of coupler **30**, the power or energy of the signal is split into two equal quantities, with one quantity fed to output port Y_1 and the other fed to output port Y_2. The signal phase of the power transmitted from output port Y_2 is delayed by 90 electrical degrees, or one-quarter of an operating wavelength, from the signal phase of the power transmitted from output port Y_1. Similarly, if the power of signal B is received at input port B, the power of the signal is split into two equal quantities, with half of the power fed to output port Y_1 and the other half fed to output port Y_2. And the signal phase of the power from signal B transmitted from output port Y_1 is delayed by 90 electrical degrees, or one-quarter of an operating wavelength, from the signal phase of the power transmitted from output port Y_2.

Thus, if signal A is applied to input port A, and signal B applied to input port B, signals appearing at output ports Y_1 and Y_2 are represented by the equations below.

$$Y_1 = \frac{A}{\sqrt{2}} \angle -90° + \frac{B}{\sqrt{2}} \angle -180°$$

$$Y_2 = \frac{A}{\sqrt{2}} \angle -180° + \frac{B}{\sqrt{2}} \angle -90°$$

$$\frac{1}{\sqrt{2}} \begin{bmatrix} -j & -1 \\ -1 & -j \end{bmatrix} \begin{bmatrix} A \\ B \end{bmatrix} = \begin{bmatrix} Y_1 \\ Y_2 \end{bmatrix} \quad j \text{ is } 1\angle 90° = \text{sqrt}(-1)$$

As shown by the above equations, if signal power is simultaneously applied to input ports A and B, signal superposition occurs because the coupler is linear.

In summary, any power received at an input port is divided equally between the output ports of the coupler, and signals transmitted by the output ports have a phase difference.

There are several ways to construct coupler **30**. One way is to use shielded (double ground plane) striplines or microstriplines. This stripline coupling technique is schematically represented in FIG. **3** and described in U.S. Pat. No. 3,731,217 to Gerst et al. (1973), which is incorporated herein by reference.

With reference now to FIG. **4**, a 4×4 Fourier Transform Matrix is illustrated. As illustrated, Fourier Transform Matrix **40** includes four couplers **30** connected as shown. Such a 4×4 transform matrix has four inputs and four outputs.

FIG. **5** shows a 4×4 transform matrix known as a Butler type transform matrix. Butler matrix **50** is essentially the Fourier Transform Matrix **40** with the addition of phase shifters **52** and **54**. If phase shifters **52** and **54** are 45° phase shifters, Butler matrix **50** is referred to as a 45° Butler matrix.

Referring again to FIG. **1**, an amplifier in amplifier array **26** has a cost proportional to a design parameter referred to as a peak to average ratio. This peak to average ratio compares the peak power output capability of the amplifier to the average power the amplifier is designed to sustain. A higher peak power, which raises the peak to average ratio, requires larger or more expensive components in the amplifier. Thus, an amplifier designed for a higher peak to average ratio is more expensive and more difficult to design.

In an effort to reduce amplifier cost, amplifier designers may include a clipping circuit before the amplifier to limit the instantaneous output signal amplitude to a predetermined maximum value, regardless of the amplitude of the signal input into the clipper circuit. Thus, the clipper circuit guarantees that the input to the amplifier will never exceed a fixed amplitude, thereby preventing an overload condition. When the input signal to the amplifier is limited to this fixed amplitude, the output of the amplifier is also limited, assuming the amplifier has a fixed gain. If the amplifier output amplitude is limited to a predetermined maximum, the amplifier may be easier to design and cheaper to construct.

If hybrid matrix amplifier **20** is used in a system, such as a communications system, wherein signals on input ports I_n have a peak amplitude at different times, the problem of detecting and preventing an overload condition in amplifier array **26** becomes a complicated one. Individually limiting the power at input ports I_n using traditional methods may not prevent an overload condition in the amplifiers in the amplifier array **26**. Traditional clipping may fail because the signals at input ports I_n are divided in amplitude and shifted in phase by hybrid matrix **22** so that the signals to the amplifiers in amplifier array **26** include new combinations of signals having new peak amplitudes that result in an overload condition. This new combination of signals is not easily calculated by examining the input signals to hybrid matrix **22**.

A solution to the problem of not being able to detect an appropriate clipping level for each input would be to clip or limit the input signal at a lower level so that an overload condition is less likely to occur in amplifier array **26**. However, this additional clipping decreases the quality of the signal being amplified.

The quality can be quantified by a quality factor ρ. The ρ quality factor is defined by:

$$\rho = \frac{E^2(xy^*)}{E(x^2)E(yy^*)}$$

where x is the original real signal, y=I+jQ (the complex I and Q clipped signal), and y^* is the complex conjugate of y. According to a standard promulgated by the Telecommunications Industries Association/Electronic Industries Association/Interim Standard-95 (TIA/EIA/IS-95) entitled *Mobile Station-Base Station Compatibility Standard for Dual Mode Wide Band Spread Spectrum Cellular System*, July 1993, the signal quality factor ρ must exceed 94.9% (measured at the receiver).

Therefore, a need exists for a method and system for preventing an amplifier overload condition in a hybrid matrix amplifier array without overly reducing the quality factor of the amplified signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a high-level depiction of a prior art hybrid matrix amplifier;

FIG. 2 is a schematic representation of a prior art coupler used in a transform matrix;

FIG. 3 is a high-level pictorial representation of the prior art coupler in FIG. 2;

FIG. 4 is a high-level schematic representation of a prior art Fourier Transform Matrix;

FIG. 5 is a high-level block diagram of a prior art Butler Transform Matrix;

FIG. 6 is a block diagram of a hybrid matrix amplifier incorporating the method and system for preventing an amplifier overload condition in accordance with the method and system of the present invention;

FIG. 7 is a high-level logic flowchart which illustrates the overall method of operation of the present invention;

FIG. 8 is a high-level logic flowchart which illustrates one embodiment of a portion of the flowchart of FIG. 7 in accordance with the present invention;

FIG. 9 is a high-level logic flowchart which illustrates another embodiment of a portion of the flowchart of FIG. 7 in accordance with the present invention; and

FIG. 10 is a high-level logic flowchart which illustrates a preferred embodiment of a portion of the flowchart of FIG. 7 in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

With reference now to the figures, and in particular with reference to FIG. 6, there is depicted a schematic representation of a hybrid matrix amplifier in accordance with the method and system of the present invention. As illustrated, hybrid matrix amplifier **100** includes transform matrix **102**, which has output ports coupled to amplifier array **104**. The outputs of amplifier array **104** are coupled to input ports of inverse transform matrix **106**. In the embodiment shown in FIG. 6, transform matrix **102** and inverse transform matrix **102** are 4×4 transform matrices having four inputs and four outputs. It should be understood that transform matrix **102** and inverse transform matrix **106** need not be square matrices, and any size matrix larger than a 2×2 matrix may be selected. Thus, matrices **102** and **106** may be n×m transform matrices.

Transform matrix **102** and inverse transform matrix **106** may be implemented with different types of matrices. For example, a Fourier transform matrix or a Butler transform matrix may be used. Additionally, other transform matrices that distribute signal power from one input to multiple outputs in various phase relationships may be used.

Amplifiers in amplifier array **104** receive a low level input signal and output a high level signal that substantially matches the input signal. Amplifier array **104** may be implemented with amplifiers sold under part number "MHW927B" by Motorola, Inc., of Schaumburg, Ill., 60196. For best performance, the amplifiers in amplifier array **104** should be matched in gain and phase delay.

Because a Fourier or Butler transform matrix may be used as its own inverse matrix, inverse transform matrix **106** is typically the same type and size as transform matrix **102**. In hybrid matrix amplifier **100**, the purpose of inverse transform matrix **106** is to separate the amplified signals into discrete output signals. Thus, a signal input into transform matrix **102** may be refocused to a particular output of inverse transform matrix **106**.

Transform matrix **102** and inverse transform matrix **106** may be implemented by transform matrices similar to ones sold under part number "580014" by Anaren Microwave, Inc., in East Syracuse, N.Y., 13057.

Signals input into transform matrix **102** come from the analog outputs of D/A (digital to analog) converters **108–112**. In a CDMA communications system implemented according to the Wideband Spread Spectrum Cellular System standard EIA/TIA/IS-95, these D/A converters are implemented with a D/A converter that converts 12-bit numbers to an analog output at the rate of 4.9152 conversions per second.

Signals input into D/A converters **108–112** come from attenuators, such as clipping circuits **114–118**. Such attenuators are used to reduce the amplitude of a signal. According to an important aspect of the present invention, clipping circuits **114–118** limit the peak amplitude of input signals in response to the amplitude of the input signal in conjunction with the amplitude, or other signal characteristics, of signals input on alternate inputs of transform matrix **102**. As shown at reference numerals **120–124**, each clipping circuit **114–118** receives an input representing at least the amplitude of other input signals that will be input into transform matrix **102**.

Delay blocks **126–130** are needed to correctly synchronize all input signals as each clipping circuit **114–118** decides whether or not to clip its own input signal.

Preceding delay blocks **126–130** are estimators **132–136**. The purpose of estimators **132–136** is to measure the amplitude of the corresponding input signal. In a digital system, amplitudes may be determined by examining the bits of the digital sample, excluding the sign bit. Amplitude measurements from estimators **132–136** are coupled to overload condition detector **138**.

Overload condition detector **138** estimates that an overload condition will occur in amplifier array **106** if input signals are not clipped or otherwise attenuated by clipping circuits **114–118**. In one embodiment of the present invention, an overload condition is estimated by summing the amplitude of the input signals and comparing the sum to

a threshold, M_T. By comparing a sum to a threshold, the detection of an overload condition is more of an estimate. In other embodiments, the amplitude splitting and phase shifting that occurs in transform matrix can be considered to get a more accurate estimate of whether or not a signal input into an amplifier in amplifier array **106** will cause an amplifier overload condition.

With regard to the input signals, they are formed at summers **140–144** by summing several input signals in the form of serial streams of digital data. In a CDMA communications system, these data streams may include pilot, page, and sync channels, along with any traffic channels. These data streams are shown as MCC1–MCC20 in FIG. **6**.

In a hybrid matrix amplifier having complex input signals, the circuitry in box **170** may be implemented with the circuitry shown in block **172**. Clipping circuit **118** in block **172** is the same as in block **170**. The output of clipping circuit **118** is coupled to frequency spreaders **174**, which up-converts base band digital signals at 19.2 kilo-samples per second to 1.2288 mega-samples per second. After the up-converting process, 4X interpolator filter **176** increases the sampling rate by four times without increasing the spectrum bandwidth. Following up-converting filters **176**, digital to analog converters **178** convert IQ signals from the digital domain to the analog domain. Once the IQ signals are in the analog domain, the signals are fed into a quadrature RF up-converter, as shown at reference numerals **180** and **182**. Therefore, the output of block **172** is a radio frequency signal that conforms to the TIA/EIA/IS-95 specification at the center frequency of ω_0.

In hybrid matrix amplifier **100**, inverse transform matrix **106** is the same as transform matrix **102**. Because the same matrix is used as its inverse, input signals from D/A **108** are refocused at output **154** on inverse transform matrix **106**. Similarly, output signals from D/A **110** are refocused at output **152**, and output signals from D/A **112** are focused at output **150**. Also shown in the example of FIG. **6**, is an unused input port on transform matrix **102** that is terminated by resistor **146**. Because one input of transform matrix **102** is terminated by resistor **146**, a corresponding output of inverse transform matrix **106** must also be terminated by resistor, such as resistor **148**. Because there is no input power at the input of transform matrix **102** that is connected to resistor **146**, there should be no output power refocused at the output connected to resistor **148**.

With reference now to FIG. **7**, there is depicted a high-level flowchart that illustrates the method and operation of the present invention. As illustrated, the process begins at block **200** and thereafter passes to block **202** wherein the amplitude of each input signal is determined.

Next, the process sums the absolute value of the amplitude of each input signal, as illustrated at block **204**. The amplitude of the input signals may be represented by the variable α_i.

Next, the process compares the summed amplitude to a threshold, M_T as depicted at block **206**. If the summed amplitude exceeds threshold M_T, the process modifies the amplitude of at least one of the input signals to prevent an overload condition in the hybrid matrix amplifier, as illustrated at block **208**.

FIGS. **8**, **9**, and **10**, along with their descriptions below, describe different embodiments of the operation depicted in block **208** of FIG. **7**.

With reference now to FIG. **8**, there is depicted the process of modifying at least one input signal amplitude to prevent amplifier overload condition in a hybrid matrix amplifier according to an embodiment of the present invention. As illustrated, the process starts at block **220** and thereafter proceeds to block **222**. As illustrated at block **222** and **224**, the process attempts to locate the smallest input signal that may, by itself, be attenuated or clipped to reduce the summed amplitude to a level equal to or below threshold M_T. As depicted at block **226**, the process determines whether or not any single input signal may be clipped to eliminate an overload condition. If a single input signal α_i may be clipped, the process clips one input signal by an amount necessary to reduce the summed amplitude to a value equal or less than threshold M_T, as illustrated at block **228**. Thereafter, the process returns to block **202** in FIG. **7**, as depicted at block **230**.

If it is not possible to clip only one input signal to reduce the summed amplitude to at least threshold M_T, the process determines whether or not two input signals may be reduced in magnitude to reduce the sum amplitude to a value equal to or less than threshold M_T. As illustrated in block **232** and **234**, the process selects the two smallest input signals that may be used to reduce the sum amplitude. As depicted at block **236**, the process determines whether or not two input signals may be reduced in amplitude to reduce the summed amplitude to a value equal to or less than threshold M_T. If only two channels may be reduced in amplitude to prevent the overload condition, the two input signals having the smallest combined amplitude are selected and reduced in magnitude by an equal amount, as illustrated at block **238**. Following the clipping of the two selected input signals that allow the amplitude to be reduced below the threshold, the process returns to block **202** in FIG. **7**, as depicted at block **240**.

If, at block **236**, the process determines that no two input signals may be reduced in amplitude by a combined value large enough to reduce the summed amplitude to a value equal to a below threshold M_T, the process selects the largest of the three input signals, as illustrated at block **242**. Thereafter, the process sets the largest of the three input signals equal to a value that is half of threshold M_T, and sets the other two input signals to a value equal to one-quarter of a threshold M_T, as depicted at block **244**. Thus, the largest signal is clipped the most if it is necessary to clip all three input signals. In this embodiment, the largest signal remains the largest signal after the clipping operation.

Following the clipping of all three input signals at block **244**, the process returns to block **202** in FIG. **7**, as illustrated at block **240**.

To summarize the operation of the embodiment shown in FIG. **8**, the process locates the minimum number of input signals that can be clipped or attenuated by a value to reduce the summed amplitude to a value equal to or below threshold M_T. If no single input channel can be clipped by an amount large enough to reduce the summed amplitude to a value equal to or below threshold M_T, the process tries to find two channels with the smallest combined of two channels that may be reduced to a calculated amplitude to prevent an overload condition. If no two input signals can be reduced to prevent the overload condition, the process replaces the amplitude of all three input signals with calculated amplitudes, where the largest input signal is set to a larger value.

With reference now to FIG. **9**, there is depicted a second embodiment of the method and system for modifying signal amplitudes to prevent an overload condition in a hybrid matrix amplifier according to the present invention. As depicted, the process begins at block **260**, and thereafter

passes to block 262 wherein the process sorts the input signals by amplitude. In this example, letters A, B, and C represent the amplitude of the input signals, wherein A represents the input signal with the highest amplitude and C represents the power of the signal with the lowest amplitude. At blocks 264 and 266, the process determines whether or not all three input signals may be reduced equally by an amount necessary to reduce the summed amplitude to a value equal to or less than threshold M_T.

If all three input signals may be reduced by the same amount to prevent an overload condition, the process calculates the amount that will be subtracted from each input signal amplitude, as illustrated at block 268. Thereafter, all input signals are reduced by the same amount, as depicted at block 270. After eliminating the overload condition, the process returns to block 202 of FIG. 7, as illustrated at block 272.

With reference again to block 266, if the amplitude of one signal is small and three input signals cannot be reduced by the same amount, the process determines whether or not the overload condition can be eliminated by reducing the two most powerful signals by the same amount while setting the least powerful signal to zero, as illustrated at blocks 274 and 276.

If the two most powerful signals may be reduced by the same amount in and a third least powerful signal reduced to zero, the process determines the magnitude of the input signal reduction, Δ1, as depicted at block 278. After calculating Δ1, the process reduces the two most powerful signals by the value of Δ1, and sets the value of the least powerful input signal to zero, as illustrated at block 280. After clipping the two most powerful input signals and setting the least powerful signal to zero, the process returns to block 202 in FIG. 7, as depicted at block 272.

Referring to block 276, if the process determines that the two signals with the greatest amplitude cannot be reduced in magnitude equally to eliminate the overload condition, the process sets the highest amplitude signal equal to threshold M_T and sets the other two input signals equal to zero, as depicted at block 282. Thereafter, the process returns to block 202 in FIG. 7, as illustrated at block 272.

Therefore, the process illustrated in FIG. 9, or attenuates clips all three input signals evenly, even if only one signal could be clipped to eliminate and overload condition. If all three signals cannot be clipped evenly, two signals are clipped by the same amount and the signal with the least amplitude is set to zero. And finally, if two signals cannot be clipped by an equal amount, one signal is clipped and the two signals with the least amplitude are set to zero.

With reference now to FIG. 10, there is depicted a third and preferred embodiment of a process for modifying the amplitude of input signals to eliminate an overload condition in a hybrid matrix amplifier according to the present invention. As illustrated, the process begins at block 300 and thereafter passes to block 302. As illustrated in block 302, the process calculates a total amplitude by summing the absolute value of all input signals. Next, the process reduces the amplitude of all three input signals by an equal proportion, as depicted at block 304. The amount of this proportionate reduction is calculated by dividing threshold M_T by the total amplitude.

After reducing the amplitude of all three input signals proportionately, the process returns to block 202 in FIG. 7, as illustrated at block 306.

In the embodiment shown in FIG. 10, the rate of clipping or input signal modification occurs more frequently and signals are reduced by smaller amplitude, compared to the embodiments shown in FIG. 8 and 9.

Because hybrid matrix amplifier 100 is not a linear system, tests or simulations are necessary to determine which embodiment reduces the peak to average ratio for the same quality factor ρ. When ρ is set to 99.5%, the embodiment shown in FIG. 8 (clip only one signal if possible) yields a 9.57 dB peak to average ratio for three input signals, and 9.9 dB for six input signals. The embodiment shown in FIG. 9 (clip all signals by same amount if possible) yields a 9.3 dB peak to average ratio for three input signals, and 9.69 dB for six input signals (ρ=99.5%). And, the preferred embodiment shown in FIG. 10 (clip all inputs proportionately) produces a 9.1 dB peak to average ratio for three input signals and a 9.28 dB ratio for six input signals (ρ=99.5%). Under the same test circumstances, but without clipping, the peak to average ratio was 11.17 dB for a three input hybrid matrix amplifier and 10.58 dB for a six input hybrid matrix amplifier.

Although the embodiments for preventing amplifier overload condition shown in FIGS. 8 and 9, are illustrated with an example using three input signals, embodiments using additional input signals may be implemented. For example, if six input signals are used, the six input signals may be divided into two three input signal blocks, each with its own threshold level, such as M_a and M_b, such that $M_T=M_a+M_b$. Two three-input signal blocks are used because six input signals greatly increases the complexity of clipping circuits 114–118 in FIG. 6. Complexity increases because each clipping circuit 114–118 would receive signal amplitude information from five other input signals which would then be used to determine the appropriate clipping level at each channel.

The foregoing description of a preferred embodiment of the invention has been presented for the purpose of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications or variations are possible in light of the above teachings. The embodiment was chosen and described to provide the best illustration of the principles of the invention and its practical application, and to enable one of ordinary skill in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

What is claimed is:

1. A method for preventing an amplifier overload condition in a hybrid matrix amplifier array comprising the steps of:

measuring signal amplitude of each of a plurality of input signals;

in response to said signal amplitude measurements, estimating an overload condition that will result in an amplifier overload in said hybrid matrix amplifier array; and

in response to estimating said overload condition, modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition in said hybrid matrix amplifier array.

2. The method for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 1 wherein said step of estimating an overload condition that will result in an amplifier overload in said hybrid matrix amplifier array includes detecting that the sum of an absolute value of each of said measured signal amplitudes exceeds an overload threshold.

3. The method for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 1 wherein said step of modifying said signal amplitude of at least one of said plurality of input signals to prevent said

overload condition includes reducing the amplitude of a minimum number of input signals that can be reduced in amplitude to prevent said overload condition.

4. The method for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 1 wherein said step of modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes reducing the amplitude of a lowest amplitude input signal that can be reduced in amplitude to prevent said overload condition.

5. The method for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 3 wherein said step of modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes reducing the amplitude of a group of input signals, wherein said group of input signals includes the minimum number of input signals with the minimum summed amplitude that can be reduced to eliminate said amplifier overload condition.

6. The method for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 1 wherein said step of modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes reducing the amplitude of all of said input signals to prevent said overload condition.

7. The method for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 1 wherein said step of modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes proportionately reducing the amplitude of all of said input signals to prevent said overload condition.

8. A system for preventing an amplifier overload condition in a hybrid matrix amplifier array comprising:

means for measuring signal amplitude of each of a plurality of input signals;

means for estimating an overload condition that will result in an amplifier overload in said hybrid matrix amplifier array in response to said signal amplitude measurements; and

means for modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition in said hybrid matrix amplifier array in response to estimating said overload condition.

9. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 8 wherein said means for estimating an overload condition that will result in an amplifier overload in said hybrid matrix amplifier array includes means for detecting that the sum of an absolute value of each of said measured signal amplitudes exceeds an overload threshold.

10. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 8 wherein said means for modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes means for reducing the amplitude of a minimum number of input signals that can be reduced in amplitude to prevent said overload condition.

11. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 8 wherein said means for modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes means for reducing the amplitude of a lowest amplitude input signal that can be reduced in amplitude to prevent said overload condition.

12. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 10 wherein said means for modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes means for reducing the amplitude of a group of input signals, wherein said group of input signals includes the minimum number of input signals with the minimum summed amplitude that can be reduced to eliminate said amplifier overload condition.

13. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 8 wherein said means for modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes means for reducing the amplitude of all of said input signals to prevent said overload condition.

14. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 8 wherein said means for modifying said signal amplitude of at least one of said plurality of input signals to prevent said overload condition includes means for proportionately reducing the amplitude of all of said input signals to prevent said overload condition.

15. A system for preventing an amplifier overload condition in a hybrid matrix amplifier array comprising:

a plurality of input signal amplitude estimators, each serially coupled to a plurality of input signals;

a hybrid matrix amplifier array overload condition detector coupled to each of said plurality of input signal power estimators for producing an overload condition signal in response to detecting an amplifier overload condition; and

at least one attenuator serially coupled to one of said input signals for reducing the power of said input signal in response to said overload condition signal, wherein said amplifier overload condition is eliminated.

16. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 15 wherein said hybrid matrix amplifier array overload condition detector includes:

a summer for producing a total amplitude signal equal to the sum the absolute values of all input signal amplitudes received from said input signal amplitude estimators; and

a comparator for indicating an amplifier overload condition in response to said total amplitude signal exceeding a threshold.

17. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 15 wherein said at least one attenuator is a clipping circuit that includes means for reducing the amplitude of said serially coupled input signal in response to said overload condition signal and amplitudes of others of said plurality of input signals.

18. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 15 wherein each of said plurality of input signals is a series of digital samples.

19. The system for preventing an amplifier overload condition in a hybrid matrix amplifier array according to claim 15 wherein each of said plurality of input signals is serially coupled to one of said attenuators, and each of said attenuators includes amplitude attenuation means for reducing the amplitude of each of said plurality of input signals by a proportionate amount to eliminate said amplifier overload condition.

* * * * *

NOTICE OF OFFICE PLAN TO CEASE SUPPLYING COPIES OF CITED U.S. PATENT REFERENCES WITH OFFICE ACTIONS, AND PILOT TO EVALUATE THE ALTERNATIVE OF PROVIDING ELECTRONIC ACCESS TO SUCH U.S. PATENT REFERENCES

Summary

The United States Patent and Trademark Office (Office or USPTO) plans in the near future to: (1) cease mailing copies of U.S. patents and U.S. patent application publications (US patent references) with Office actions except for citations made during the international stage of an international application under the Patent Cooperation Treaty and those made during reexamination proceedings; and (2) provide electronic access to, with convenient downloading capability of, the US patent references cited in an Office action via the Office's private Patent Application Information Retrieval (PAIR) system which has a new feature called "E-Patent Reference." Before ceasing to provide copies of U.S. patent references with Office actions, the Office shall test the feasibility of the E-Patent Reference feature by conducting a two-month pilot project starting with Office actions mailed after December 1, 2003. The Office shall evaluate the pilot project and publish the results in a notice which will be posted on the Office's web site (www.USPTO.gov) and in the Patent Official Gazette (O.G.). In order to use the new E-Patent Reference feature during the pilot period, or when the Office ceases to send copies of U.S. patent references with Office actions, the applicant must: (1) obtain a digital certificate from the Office; (2) obtain a customer number from the Office, and (3) properly associate applications with the customer number. The pilot project does not involve or affect the current Office practice of supplying paper copies of foreign patent documents and non-patent literature with Office actions. Paper copies of references will continue to be provided by the USPTO for searches and written opinions prepared by the USPTO for international applications during the international stage and for reexamination proceedings.

Description of Pilot Project to Provide Electronic Access to Cited U.S. Patent References

On December 1, 2003, the Office will make available a new feature, E-Patent Reference, in the Office's private PAIR system, to allow more convenient downloading of U.S. patents and U.S. patent application publications. The new feature will allow an authorized user of private PAIR to download some or all of the U.S. patents and U.S. patent application publications cited by an examiner on form PTO-892 in Office actions, as well as U.S. patents and U.S. patent application publications submitted by applicants on form PTO/SB08 (1449) as part of an IDS. The retrieval of some or all of the documents may be performed in one downloading step with the documents encoded as Adobe Portable Document format (.pdf) files, which is an improvement over the current page-by-page retrieval capability from other USPTO systems.

Steps to Use the New E-Patent Reference Feature During the Pilot Project and Thereafter

Access to private PAIR is required to utilize E-Patent Reference. If you don't already have access to private PAIR, the Office urges practitioners, and applicants not represented by a practitioner, to take advantage of the transition period to obtain a no-cost USPTO Public Key Infrastructure (PKI) digital certificate, obtain a USPTO customer number, associate all of their pending and new application filings with their customer number, install no-cost software (supplied by the Office) required to access private PAIR and E-Patent Reference feature, and make appropriate arrangements for Internet access. The full instructions for obtaining a PKI digital certificate are available at the Office's Electronic Business Center (EBC) web page at: <http://www.uspto.gov/ebc/downloads.html>. Note that a notarized signature will be required to obtain a digital certificate.

To get a Customer Number, download and complete the Customer Number Request form, PTO-SB125, at: http://www.uspto.gov/web/forms/sb0125.pdf. The completed form can then be transmitted by facsimile to the Electronic Business Center at (703) 308-2840, or mailed to the address on the form. If you are a registered attorney or patent agent, then your registration number must be associated with your customer number. This is accomplished by adding your registration number to the Customer Number Request form. A description of associating a customer number with an application is described at the EBC web page at: http://www.uspto.gov/ebc/registration_pair.html.

The E-Patent Reference feature will be accessed using a new button on the private PAIR screen. Ordinarily all of the cited U.S. patent and U.S. patent application publication references will be available over the Internet using the Office's new E-Patent Reference feature. The size of the references to be downloaded will be displayed by E-Patent Reference so the download time can be estimated. Applicants and registered practitioners can select to download all of the references or any combination of cited references. Selected references will be downloaded as complete documents as Adobe Portable Document Format (.pdf) files. For a limited period of time, the USPTO will include a copy of this notice with Office actions to encourage applicants to use this new feature and, if needed, to take the steps outlined above in order to be able to utilize this new feature during the pilot and thereafter.

During the two-month pilot, the Office will evaluate the stability and capacity of the E-Patent Reference feature to reliably provide electronic access to cited U.S. patent and U.S. patent application publication references. While copies of U.S. patent and U.S. patent application publication references cited by examiners will continue to be mailed with Office actions during the pilot project, applicants are encouraged to use the private PAIR and the E-Patent Reference feature to electronically access and download cited U.S. patent and U.S. patent application publication references so the Office will be able to objectively evaluate its performance. The public is encouraged to submit comments to the Office on the usability and performance of the E-Patent Reference feature during the pilot. Further, during the pilot period registered practitioners, and applicants not represented by a practitioner, are encouraged to experiment with the feature, develop a proficiency in using the feature, and establish new internal processes for using the new access to the cited U.S. patents and U.S. patent application publications to prepare for the anticipated cessation of the current Office practice of supplying copies of such cited

references. The Office plans to continue to provide access to the E-Patent Reference feature during its evaluation of the pilot.

Comments

Comments concerning the E-Patent Reference feature should be in writing and directed to the Electronic Business Center (EBC) at the USPTO by electronic mail at eReference@uspto.gov or by facsimile to (703) 308-2840. Comments will be posted and made available for public inspection. To ensure that comments are considered in the evaluation of the pilot project, comments should be submitted in writing by January 15, 2004.

Comments with respect to specific applications should be sent to the Technology Centers' customer service centers. Comments concerning digital certificates, customer numbers, and associating customer numbers with applications should be sent to the Electronic Business Center (EBC) at the USPTO by facsimile at (703) 308-2840 or by e-mail at EBC@uspto.gov.

Implementation after Pilot

After the pilot, its evaluation, and publication of a subsequent notice as indicated above, the Office expects to implement its plan to cease mailing paper copies of U.S. patent references cited during examination of non provisional applications on or after February 2, 2004; although copies of cited foreign patent documents, as well as non-patent literature, will still be mailed to the applicant until such time as substantially all applications have been scanned into IFW.

For Further Information Contact

Technical information on the operation of the IFW system can be found on the USPTO website at http://www.uspto.gov/web/patents/ifw/index.html. Comments concerning the E-Patent Reference feature and questions concerning the operation of the PAIR system should be directed to the EBC at the USPTO at (866) 217-9197. The EBC may also be contacted by facsimile at (703) 308-2840 or by e-mail at EBC@uspto.gov.

Date. 12/1/03

Nicholas P. Godici

Nicholas P. Godici
Commissioner for Patents

USPTO TO PROVIDE ELECTRONIC ACCESS TO CITED U.S. PATENT REFERENCES WITH OFFICE ACTIONS AND CEASE SUPPLYING PAPER COPIES

In support of its 21st Century Strategic Plan goal of increased patent e-Government, beginning in June 2004, the United States Patent and Trademark Office (Office or USPTO) will begin the phase-in of its E-Patent Reference program and hence will: (1) **provide downloading capability of the U.S. patents and U.S. patent application publications cited in Office actions** via the E-Patent Reference feature of the Office's Patent Application Information Retrieval (PAIR) system; and (2) **cease mailing paper copies of U.S. patents and U.S. patent application publications with Office actions** (in applications and during reexamination proceedings) except for citations made during the international stage of an international application under the Patent Cooperation Treaty (PCT). In order to use the new E-Patent Reference feature applicants must: (1) obtain a digital certificate and software from the Office; (2) obtain a customer number from the Office; and (3) properly associate patent applications with the customer number. Alternatively, copies of all U.S. patents and patent application publications can be accessed without a digital certificate from the USPTO web site, from the USPTO Office of Public Records, and from commercial sources. The Office will continue the practice of supplying paper copies of foreign patent documents and non-patent literature with Office actions. Paper copies of cited references will continue to be provided by the USPTO for international applications during the international stage.

Schedule

June 2004	TCs 1600, 1700, 2800 and 2900
July 2004	TCs 3600 and 3700
August 2004	TCs 2100 and 2600

All U.S. patents and U.S. patent application publications are available on the USPTO web site. However, a simple system for downloading the cited U.S. patents and patent application publications has been established for applicants, called the E-Patent Reference system. As E-Patent Reference and Private PAIR require participating applicants to have a customer number, retrieval software and a digital certificate, all applicants are strongly encouraged to contact the Patent Electronic Business Center to acquire these items. To be ready to use this system by June 1, 2004, contact the Patent EBC as soon as possible by phone at 866-217-9197 (toll-free), 703-305-3028 or 703-308-6845 or electronically via the Internet at ebc@uspto.gov.

Other Options

The E-Patent Reference function requires the applicant to use the secure Private PAIR system, which establishes confidential communications with the applicant. Applicants using this facility must receive a digital certificate, as described above. Other options for obtaining patents which do not require the digital certificate include the USPTO's free Patents on the Web program (http://www.uspto.gov/patft/index.html). The USPTO's Office of Public Records also supplies copies of patents for a fee (http://ebiz1.uspto.gov/oems25p/index.html). Commercial sources also provide U.S. patents and patent application publications.

For complete instructions see the Official Gazette Notice, USPTO TO PROVIDE ELECTRONIC ACCESS TO CITED U.S. PATENT REFERENCES WITH OFFICE ACTIONS AND CEASE SUPPLYING PAPER COPIES, on the USPTO web site.